RF and Microwave Filter Design By Means of Single Transistor Active Inductor: a Review

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Abstract — RF and Microwave active filters design by the use of grounded active inductor (AI) is here presented. The proposed single transistor AI emulates an inductor behaviour by implementing a passive variable phase and amplitude compensating network and amplifiers, forming a similar gyrator-C architecture allowing its use in LC filters architectures at high frequencies with high quality factor and reduced occupied chip area. The design method can be applied with success, in particular, for the design of bandpass filters with very high performances in terms integration and application from RF to Microwave frequency range achieving active filters with relatively high dynamic range, constant Q and also easy frequency tuning capability.

Index Terms — Filters, Active Filters, Active inductor.

I. INTRODUCTION

RECENT advancements in integrated circuits (IC) and communications systems, in conjunction with the great increasing request for miniaturisation and size reduction of wireless systems and devices, have led to an increase of performances and space reduction of modern telecommunication apparatus. As a consequence most RF and microwave system blocks have been successfully implemented as IC with different technologies. In this scenario, analog tunable filters working, in general, at RF and microwave frequencies still remain the most difficult part to be integrated in a single chip [1-10], due to requirements in input and output impedance matching, stability, and dynamic range and noise. In fact most commercial wireless receivers only use off-chip filters that are typically implemented with discrete components, being in IC circuits most of the semiconductor area occupied by passive elements, while active devices play a marginal role in area occupation. Spiral inductors, in fact, require large amounts of substrate area, have limited bandwidth, high series resistance, and crosstalk problems. In this scenario, in the last decades Active Inductors (AI) [11-20] have demonstrated to be good candidates for high-frequency operation, therefore. considerable interest has been shown in their use in active filters. In this perspective, in particular, band-pass filters

designed by means of active inductor, usually suffer from a very low dynamic range due to the combination of a high noise level introduced by the AI and the relatively low compression power level of the AI itself. For all these reasons there are only a few commercial solutions available on the market based on active inductors. Based on the same author experience in the field [21-39], this work describes an approach to design single transistor active inductor based filters characterized by high quality factor and high dynamic power range. As an example application already developed a RF bandpass filter is also reported and discussed both at IC and discrete element board level.

II. THE SINGLE TRANSISTOR AI

The first high-Q AIs were reported over two decades ago and the use of these inductors for the implementation of *L*-*C* resonator-type active filters was presented both in several papers and conferences. The classical gyrator-C architecture, as shown in Figure 1, is the most well-known method to design an AI.

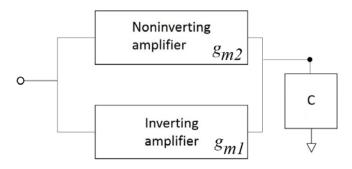


Fig. 1. Classical Gyrator-C Structure

In this case the equivalent inductance of the gyrator-based active inductor can be expressed as:

$$L_{eq} = \frac{C}{g_{m1}g_{m2}} \tag{1}$$

If we consider a real case non idealities in the amplifiers must be taken into account and two unwanted effects appears. In particular a parasitic resistance arises in series to the

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equivalent inductance and the bandwidth of the inductive impedance becomes finite. Fig. 2 shows that a phase relation between voltage and current at the system input less than 90° gives positive resistance, while a phase relation in excess of 90° causes a negative resistance.

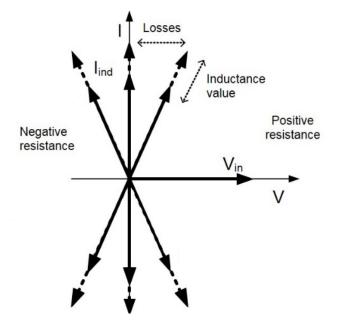


Fig. 4. Simplified schematic model of the single-transistor AI.

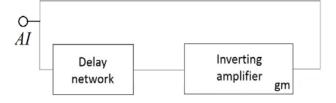
Now it can be seen that the input impedance of the network is not always inductive. By analysing the imaginary part we can notice that the imaginary part of the AI impedance has a zero in ω =0, and it is always positive only if:

$$g_m R > l \tag{3}$$

Moreover, the imaginary part of the input impedance is monotonically growing, thus inductive, until its maximum is reached for:

$$\omega_{max} = \sqrt{\frac{g_m^2 - Rg_m^3}{C^2 - Rg_m C^2}} \tag{4}$$

The high-Q condition has been explained conceptually on the IV-plane with complex phasors (see Fig. 2) in order to clarify the Active Inductor behaviour and characteristics. Surely, a mathematical analysis can be compliant and equations can be obtained. Anyway, even if equations can be written considering the equivalent circuits, it is not straightforward to obtain useful design formulas due to the presence of the feedback loop. Anyway, the equivalent circuit in Fig. 5 has been analysed and the expression of the input impedance is shown in eq. (4).



If we were able to control both these phase relations, without

acting on the bias condition of the amplifiers, the linearity of

the active component of the gyrator will not be affected. This

condition can be reached by the insertion of a suitable variable

passive compensation network, moreover, in order to simplify

the design, a single active block AI with a compensation

network can be also adopted as shown in Fig. 3. In this case a

simplified model of the capacitance gyrator with a single

Fig. 3. Single active block AI block scheme

Fig. 2. AI voltage and current relations

active block is designed.

In the ideal case starting from Fig. 3 block scheme and, considering the simplified Fig. 4 equivalent circuit linear model of a single transistor AI, the circuit input impedance is given by the following relation:

$$Z_{in} = \frac{1 + j\omega RC}{g_m + j\omega C}$$
(2)

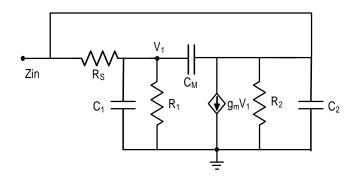


Fig. 5. Simplified schematic model of the single-transistor AI considering also transistor parasitics

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{\left(1 + \frac{R_S}{R_1} + sC_MR_S + sC_1R_S\right)}{\frac{1}{R_1} + \frac{R_S}{R_2} + g_m\frac{R_S}{R_1R_2} + s\left(C_1 + C_2 + C_M\frac{R_S}{R_2} + C_1\frac{R_S}{R_2} + g_mC_MR_S + C_M\frac{R_S}{R_1} + C_2\frac{R_S}{R_1}\right) + s^2(C_MC_2R_S + C_1C_2R_S + C_MC_1R_S)}$$
(5)

The AI high Q behaviour can now be obtained by zeroing the real part of the input impedance at the desired frequency being it calculated as $Q=\omega L/R$ (where L=Img(Zin) and R=Re(Zin)). As it is evident form eq. (5), due to the non-general formulation of the problem, the problem can be solved easier if treated with a numerical approach.

Anyway, in any case general design considerations can be still done. The use of highly linear devices, the use low-pass filter topology compensating network, the use of high precision passive components with high quality factors are general rules that allow to obtain a suitable design.

III. FILTERS EXAMPLE APPLICATIONS

As general examples it is here reported both an integrated and discrete solution implemented at 2GHz and already presented and discussed in []. In both cases the simple LC structure depicted in Fig 6. is applied for the designed filter.

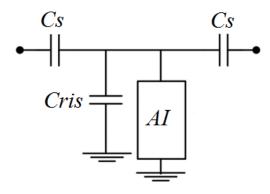


Fig. 7. Bandpass filter architecture.

As reported in [21], "the IC (using a 0.25um BiCMOS technology) AI implementation of the transconductance amplifier, see Fig. 8, is achieved by means of a commonemitter configuration, biased through the resistances *Rb* and *Rc*. The power dissipation is about 80µW biasing with a 1.2V power supply voltage. C_{DCB} capacitances are DC block while the capacitances C_{1-2} and resistances R_{1-2} form the compensation network. The topology of the compensating network and its components value, have been chosen in order to have an inductive behavior with minimum non-negative series resistance around 2000 MHz, providing a very high quality factor. In fact, simulated results of the applied bandpass filter give the S-parameter response depicted in Fig. 9. The filter is centered at 2 GHz with an insertion loss of 0.5dB and it has a 3dB bandwidth of about 6MHz with a quality factor of about 330. Both input and output matching are lower of -15dB".

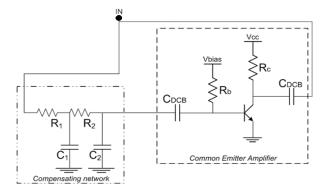


Fig. 8. Single-transistor AI detailed schematic circuit [21].

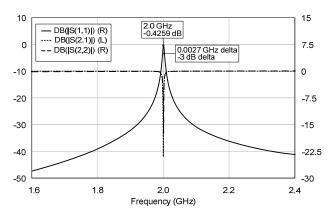


Fig. 9 . Simulated S parameter response [21].

A discrete prototype board also presented in [21] is here reported being designed with a similar design approach. Figure 10 shows in the right upside the fabricated PCB: the amplifier is based on the BFP420 BJT from Infineon, in common-emitter configuration. Finally always in Fig. 10 it is shown the measured and simulated S parameters of the filter. The 3dB bandwidth is about 10MHz; it shows a P1dB compression point of -10dBm with a power supply voltage of 1.2V and a power consumption of 0.8mW. The noise figure (NF) of the circuit at 2000 MHz is approx. 6 dB.

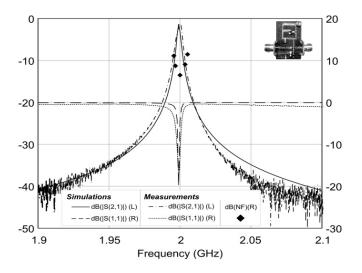


Fig. 10. PCB photo and measured and simulated S_{21} and S_{11} , together with the measured noise figure of the discrete element filter [21].

IV. CONCLUSION

We have here addressed a general review of RF and Microwave active filters design method by the use of a single transistor grounded active inductor (AI). The AI is composed by only a passive variable phase and amplitude compensating network and a single transistor amplifier, forming a similar gyrator-C architecture. As reported in the literature the design method can be applied with success for the design of bandpass filters with very high performances in terms integration and performances.

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