Design of IIR Filters based on all-pole Critical Monotonic Amplitude Characteristic analog prototypes

Dejan Mirković, Borisav Jovanović, Miona Andrejević Stošović, Vančo Litovski and Milena Stanojlović Mirković

Abstract—**This paper presents design procedure for efficient design of IIR digital filters with critical monotonic amplitude characteristic (CMAC). Design methodology is based on traditional approach i.e. synthesizing the filter transfer function in s-domain and utilizing appropriate conformal mapping to produce z-domain transfer function. Only hardware, fixed-point, implementation is considered. Presented procedure covers design flow from system level to the register transfer level (RTL) modeling and simulation. As an example, highly selective, notch, filter is designed. Obtained simulation results confirmed proper functionality of the designed filter.**

Index Terms— **IIR filters, VHDL, RTL design.**

I. Introduction

THE electronic filter design has always been the inevitable problem to confront with over the nearly century of modern electronic revolution. Many researchers all around the globe invested tremendous intellectual effort to produce myriad of results regarding filter design problem that exist today [1-6]. This richness of results and literature makes the field of filter design somehow cumbersome and unattractive. However, real-life problems emerging either, from appearance of new technologies and concepts, or from improving the existing ones, forces engineering and research community to come back to the problem of filter design.

Today, we are all witnesses of rapid progress in both telecommunications and integrated circuit design. Namely, the number of wireless connected mobile devices is constantly increasing announcing the new revolution in telecommunication and electronics usually labeled as Internet Of Things (IoT). This trend forces providers of telecommunication services to ensure and handle huge number of separate channels in frequency domain. Therefore, a high selectivity is a must in order to protect contiguous channels from mutual aliasing. On the other hand, one of the leading constraints in the design of integrated circuits, driven by the battery life and portability of a mobile device, are power consumption and area of the silicon used to implement given functionality. Therefore, engineers have to trade-off all those constraints at various levels of abstraction in order to come up with optimal solution for target application. Since high selectivity is hard to achieve using finite impulse response (FIR) approach, utilizing infinite impulse response (IIR) concept for providing high selectivity under low power and silicon area constraint becomes more and more attractive. Unfortunately, choosing IIR concept is usually paid with distortion in phase characteristics, therefore additional phase correction circuitry is necessary to mitigate with this problem.

The goal of this paper is to supplement the rich set of already developed and successfully used techniques for designing IIR filters in order to help engineering community to cope with this matter. Paper is organized as follows.

In second section, brief recapitulation of traditional design methodology of IIR filters will be covered. The third section outlines the properties of four main classes of filter functions exhibiting Critical Monotonic Amplitude Characteristic (CMCA). In fourth section design example of the highly selective, notch, all-pole CMAC IIR filter design will be given. Special concern will be devoted to stability and rounding of filter's coefficients. Simulations results of RTL model of the filter implemented in VHDL are presented and discussed in fifth section. Conclusion will provide final thoughts and comments about proposed solution for achieving high selectivity.

II. Traditional design of IIR filters

It is well known from the literature that the traditional method for obtaining infinite impulse response (IIR) system in digital i.e. z-domain starts with synthesis of analog, s-domain, prototype, polynomial, rational transfer function. Synthesized prototype transfer function is dimensionless in frequency domain i.e. cutoff frequency is scaled to one. From this point, there are two viable methods to obtain adequate digital representation of an analog prototype. These methods are depicted in Fig. 1.

Approach shown in Fig. 1b assumes that after synthesizing low pass transfer function in s-domain, frequency translation which gives the filter with real cutoff frequency(ies) is performed also in s-domain. Second method depicted in Fig. 1b suggest that prototype analog transfer function should be first mapped in z-domain, and then to perform frequency translation, now called wrapping, in z-domain.

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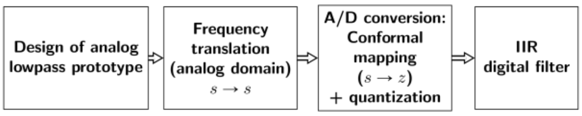
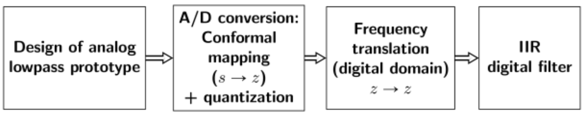


(a)



(b)

Fig. 1 Flow of digital IIR filter design based on traditional approach

In both approaches, there is a process of transforming complex frequency *s* in complex frequency *z* via adequate conformal mapping. This operation is usually known as s- to z- mapping. Through mapping operation only time is discretized. After s- to z- mapping follows quantization, i.e. discretization of the value. These two operations are commonly referred to as Analog-to-Digital (A/D) conversion. Of course, this process inevitably leads to loss of information i.e. distortions in characteristics of the initial analog system.

Therefore, z domain system obtained through this process can be observed as approximation of s-domain system. There is a number of different conformal mappings that serves this purpose. Usually they are roughly classified as the ones that tries to approximate one of the analog prototype's characteristic at the cost of neglecting the other. In this group one can classify methods such are: impulse response invariant [7], step invariant [8] or magnitude/phase-invariance methods [9, 10].

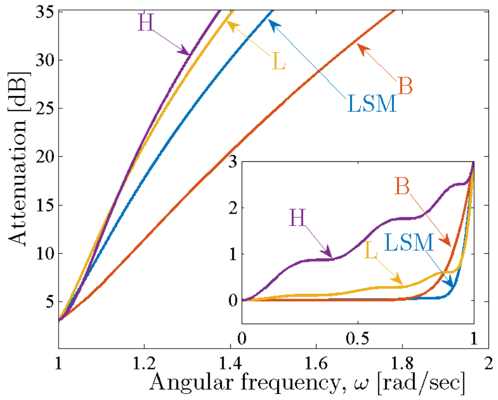
Second group includes conformal mappings that approximates the continuous time derivation (integration) operation. In this group, one can find famous Forward/Backward Euler and bilinear (Tustin) transformation [11]. These kinds of transformations usually give the best approximation of analog system's magnitude characteristic (i.e. filter's attenuation) which usually is the prime design goal. Besides this well-established, there are new transformations that tries to simultaneously approximate both phase and magnitude characteristics like the one proposed in [12].

Finally, when z-domain, IIR, filter is synthesized, it can be implemented in many possible software or hardware architectures. This work considers only structural, canonical, hardware implementation where sampling frequencies are quite high (like in modern telecommunication interfaces) and approach like multiply and accumulate (MAC) cannot be applied.

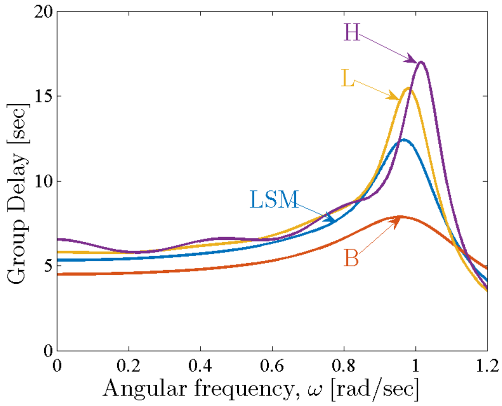
III. CMAC FILTER FUNCTIONS

For completeness, brief discussion about CMAC class of filter functions will be given. For more detailed insight reader is advised to look in [13]. Four basic classes of CMAC filter functions are:

- Butterworth (B) [4]
- Optimal-L (L) [5]
- Halpern (H) [3] and
- Least-Square Monotonic (LSM) [14]



(a)



(b)

Fig 2. Characteristic of 7th order prototypes based on CMAC filter functions: (a) attenuation and (b) group delay

In order to choose appropriate class of CMAC filter functions for given application, general comparison of four basic classes will be performed.

Attenuation and group delay characteristics of 7th order analog prototype implemented with all four classes of CMAC functions shown in Fig. 2 will be used to support this discussion. Based on Fig. 2a it can be observed that LSM filter functions provides best approximation of ideal brick-wall filter function in pass-band while maintaining the decent selectivity in stop-band. As expected H filters have largest attenuation in stop-band and L filters can be considered as compromise between H and LSM.

The most popular one, B filters, do not provide any advantages in terms of selectivity comparing to e.g. LSM, except maximal flattens of attenuation characteristic. Of course, when looking in Fig. 2b B filters exhibit smallest group delay in pass-band. When group delay is observed, now LSM can be viewed as the trade-off between L and B filters. Generally, it can be concluded that LSM filters provide best compromise between group delay, selectivity and monotonicity of attenuation characteristic. Therefore, LSM filter prototype is to be exploited in following design example.

IV. DESIGN EXAMPLE

Highly selective, band-reject, i.e. notch IIR digital filter is designed in order to prove good selectivity properties of the

LSM filter functions. This example is chosen because it is used quite often in Multi Standard Radio (MSR) base stations.

In MSR systems sampling frequency is usually defined as f_s=61.44MHz. Practically, one design parameter i.e. sampling frequency is already known.

Design requirements are: central frequency f_0=5MHz, stop-band f_b=2MHz and at least 60dB of attenuation at f_0. This attenuation can be achieved with 4th order LSM prototype. Since approach shown in Fig. 1a is adopted, analog low-pass prototype is translated to equivalent band-reject before s- to z-mapping. This is done using the relation given in (1).

$$\omega \leftarrow BW_r \frac{\Omega_0 \Omega}{\Omega_0^2 - \Omega^2} \tag{1}$$

In (1) $BW_r = f_b/f_0$ is relative bandwidth, $\Omega_0 = 2\pi f_0$, Ω is real, translated, angular frequency and ω is normalized angular frequency of analog porotype [15]. Poles of 4th order LSM prototype, and translated 8th order band-reject analog filters are given in Table I. Of course, according to (1) resulting band-reject filter have four pairs of complex-conjugate zeros at $\pm j\Omega_0$.

TABLE I POLES OF THE 4TH ORDER LSM LOW-PASS PROTOTYPE AND 8TH ORDER BAND-REJECT FILTERS

No.	Low-pass	Band-reject*
1/2	-0.2838434341 $\pm j$0.9265437853	-0.0487295044 $\pm j$0.8202217798
3/4	-0.6886065659 $\pm j$0.3750262747	-0.1961900822 $\pm j$0.8605934781
5/6		-0.2518125277 $\pm j$1.1045829462
7/8		-0.0721770666 $\pm j$1.2148944003

* Poles are normalized with Ω_0

Because linear phase is not of prime concern in this design, bilinear transform is exploited for s- to z- mapping of analog prototype into digital domain.

For system level design automation, MATLAB scripts were used. Since synthesis of LSM filter functions is not available in MATLAB's signal-processing toolbox (or any other software package for numerical/symbolic analysis), C implementation of the LSM algorithm is written based on [14] and [13]. Results of the C routine for synthesizing all-pole LSM filter functions are further used in conjunction with custom-written MATLAB scripts to automate the whole process of designing the IIR filter based on LSM prototype.

A. Filter architecture

When designing higher order IIR filters one must choose between cascade or parallel architecture in order to minimize influence of finite precision of filter's coefficients representation. Even cascade realization is popular for IIR filter realization, parallel realization proves to be more resilient to finite precision of coefficients representation as shown in e.g. [16].

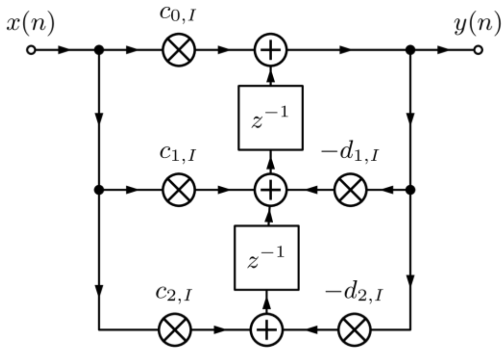


Fig. 3 Transpose direct form II (TDF II) of I-th 2nd order IIR filter section

Therefore, parallel realization is adopted in this work. Each of 2nd order sections of designed notch IIR filter is realized using Transpose direct form II depicted in Fig. 3. Transfer function of filter shown in Fig. 3 is given with,

$$H_I(z) = \frac{c_{0,I} + c_{1,I} z^{-1} + c_{2,I} z^{-2}}{1 + d_{1,I} z^{-1} + d_{2,I} z^{-2}}. \tag{2}$$

B. Finite precision of filter coefficients representation

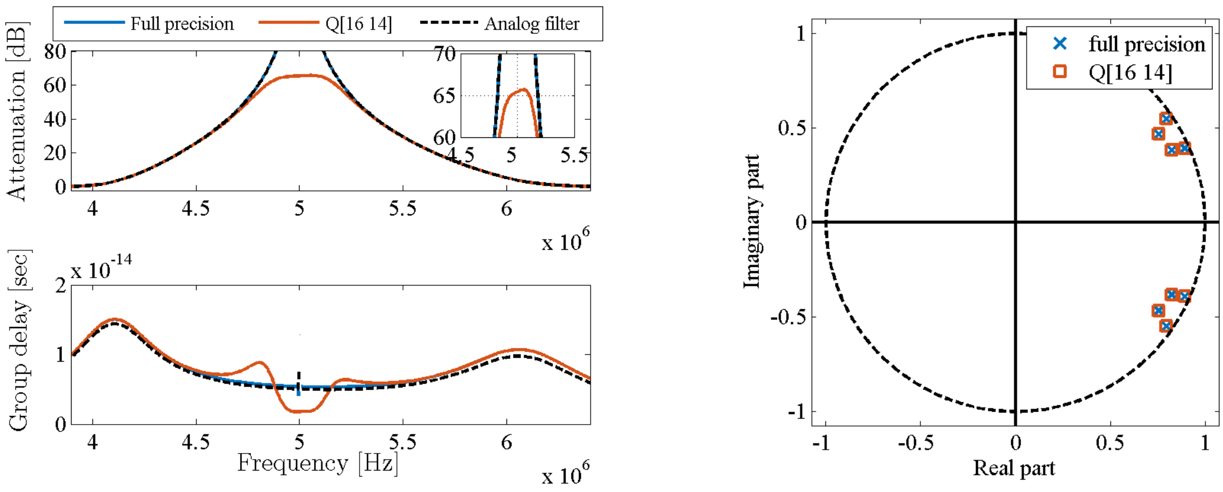
Only fixed-point precession of coefficient representation is taken into account since it is considered as standard in DSP hardware [17]. To explore influence of finite precision of coefficients representation on key filter characteristics, algorithm shown in Fig. 4 is implemented.

```
for word_length = [8, 12, 16, 24, 32]
  for I=1:number_of_sections
    quantize coefficients of …
    I-th section;
    calculate frequency response and …
    zeros/poles location of I-th section;
  end
  sum individual frequency responses;
  plot results;
end
```

Fig. 4 Pseudo-code of algorithm for exploring influence of the finite precision of coefficient representation on key filter characteristics

After set of numeric analyses are preformed, fixed-point, 16-bit representation of filter coefficients turns out to be adequate. Attenuation and group delay characteristics for analog, digital with coefficients in full-precision and digital with quantized coefficients are shown in Fig. 5a. Here full-precision is 32-bit floating point representation. Fixed-point, quantization format is marked with Q[16 14] meaning that there is 16-bits word length with 14 bits after decimal point. Full-precision and quantized filter coefficients for each section are given in Tables II and III. Hexadecimal representation is used for quantized coefficients.

When looking in Fig. 5a one can notice expected distortion in phase i.e. group delay characteristics in stop-band.



(a) (b)

Fig. 5 Characteristics of designed notch filter: (a) Attenuation and group delay of analog, digital with coefficients in full precision and digital with quantized coefficients filters and (b) Location of poles in z-plane for digital IIR filter with full precision (×) and quantized (□) coefficients.

TABLE II NUMERATOR COEFFICIENTS OF THE DESIGNED IIR 8TH ORDER NOTCH FILTER

Precision	Section	Numerator coefficients		
		c_0	c_1	c_2
Full	I	-0.016398696220208495	-0.016398696220208495	-0.016398696220208495
	II	-0.11221057157164607	-0.11221057157164607	-0.11221057157164607
	III	-0.11019287746605651	-0.11019287746605651	-0.11019287746605651
	IV	0.00015330163696891563	0.00015330163696891563	0.00015330163696891563
Q[16 14]	I	FEF3	FF4E	005B
	II	F8D2	FF58	0687
	III	F8F3	0106	0814
	IV	0003	016F	016D

TABLE III DENOMINATOR COEFFICIENTS OF THE DESIGNED IIR 8TH ORDER NOTCH FILTER

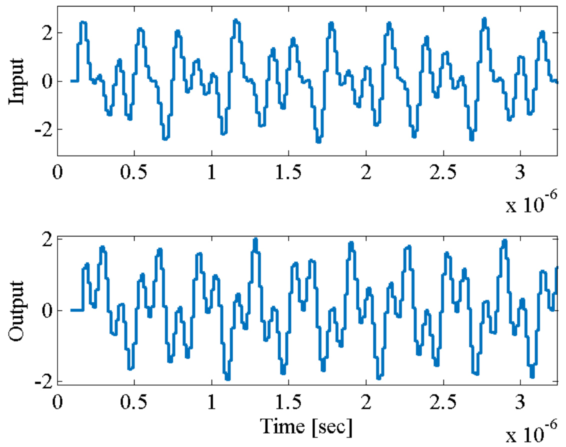
Precision	Section	Denominator coefficients	
		d_1	d_2
Full	I	-1.7882674878828715	0.95338516696825548
	II	-1.6487819031997475	0.8257235454351094
	III	-1.5109088557315891	0.78764174263605213
	IV	-1.5933094079882946	0.93489392658498971
Q[16 14]	I	8D8D	3D04
	II	967A	34D9
	III	9F4D	3269
	IV	9A07	3BD5

There is a slight increase in pass-band group delay as well. On the other hand, high selectivity and more than required 60dB attenuation at central frequency is achieved with 16-bit world length.

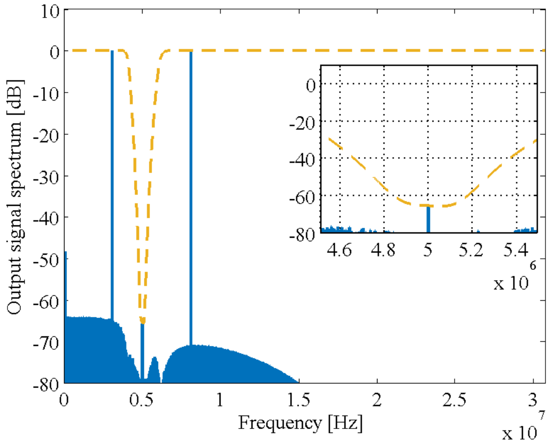
Besides attenuation and group delay characteristics, location of poles in z-plane for both full-precision and quantized coefficients of digital IIR filter sections is given in Fig. 5b. As can be seen in Fig. 5b stability is preserved affirming parallel realization robustness.

V. SIMULATION RESULTS

Finally, after architecture and quantization format for the coefficients are chosen and verified at system level, RTL model of the designed filter can be created. VHDL is chosen for implementation of RTL model of the designed filter. Appropriate test-bench is written as well. Input of the filter is excited with composite test signal given in (3).



(a)



(b)

Fig. 6 Simulation results for RTL model of IIR, 8th order, BS filter: (a) Time response and (b) Output signal spectrum.

$$a(t) = \sin(2\pi \cdot f_0 t) + \sin(2\pi \cdot f_1 t) + \sin(2\pi \cdot f_2 t) \quad (3)$$

In (3) $f1$=3.09MHz and $f2$=8.09MHz. These frequencies are chosen in such a way to be symmetric around f_0. Therefore, both sides of pass-band are covered. Simulation results of RTL model of the designed filter are presented in Fig. 6. Time response is shown in Fig. 6a and output signal spectrum in Fig. 6b. In output spectrum magnitude characteristic of the filter with quantized coefficients obtained at system level is plotted with dashed line for comparison purposes. Output signal spectrum is obtained with 2^{14} point FFT.

Observing zoomed pass-band detail in Fig. 6b one can see that required, greater then 60dB attenuation, is achieved at RTL level. Since RTL level is the closest to physical implementation, RTL model can be safely implemented in ASIC and/or FPGA. On the other hand, there is DC level of about -48dBs. This is partly result of scaling of input signal to prevent limit cycles and preserve stability [17]. Besides this, at RTL level true fixed-point arithmetic is performed. Namely, there is always truncation of data at the outputs of arithmetic blocks (adders, multipliers) which inevitably result with round-off noise.

VI. Conclusion

Concerning the need for low power consumption and high selectivity of filters used in mobile wireless applications one solution based on special class of CMAC filter functions is examined in this paper. Complete design procedure starting from analog prototype synthesis all the way to the RTL modeling and simulation is covered. Since the synthesis of LSM prototype filter functions is not available in any of commonly used software packages for numerical/symbolic analysis, a number of useful software routines implemented in C and MATLAB are written in order to provide design flow for designed filter solution. Simulation results confirmed that proposed solution can be successfully utilized in systems that require high selectivity and minimal hardware.

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