

A highly linear CMOS TIA based on triple-inverter amplifier

Dušan P. Krčum, Ivan M. Milosavljević, Đorđe P. Glavonjić, Darko M. Tasovac and Lazar V. Saranovac

Abstract— This paper presents the highly linear and low-noise transimpedance amplifier (TIA) based on CMOS inverter as an amplifier within multiple feedback (MPFB) filter topology. Absence of complex analog circuitry and compatibility with widespread digital CMOS processes highlight this TIA topology as the best choice in signal conditioning chains approaching analog-to-digital converters (ADCs). Special attention has been given to the TIA stability and compensation networks. Using dedicated low-dropout (LDO) regulator the variations in TIA performance induced by supply noise have been made more robust. Transimpedance and bandwidth programmability is ensured by design of the feedback network. Nominal transimpedance and bandwidth at 65 °C are 72 dBΩ and 5 MHz, respectively. Achieved third-order intermodulation distortion is -84 dBc, while input third-order intercept point is 34 dBm. This performance is comparable with state of the art TIA solutions used in optical receivers and communication baseband circuits.

Index Terms—TIA, MPFB filter, triple-inverter amplifier, 65 nm CMOS, optical receivers, current mixers

I. INTRODUCTION

HIGH data rates, wide bandwidths, and low distortion levels are strictly required in many modern communication systems. Fast growing industry of augmented reality requires specific hardware that enables usage of the 3D cameras and data fusion from multiple optical receivers. All these systems need highly linear and CMOS compatible ADC interfaces. Traditional ADC interfaces for optical systems owe their outstanding performance to their hybrid nature. Namely, signal conditioning chains are usually built in different process technology than the optical systems. Given approach leads to usage dedicated bipolar transistor based topologies of the critical circuitry, however, this causes the rise in overall price of the system. Although integrated circuits for communication have better performance in the bipolar technology, mass production, high level of integration, and product price require a shift to standard digital CMOS process. This paper describes transimpedance amplifier – a block that can be used in communication systems and that is almost irreplaceable in optical sensors read-out circuitry. The presented TIA is designed in 65 nm standard CMOS process which is still good enough for integration of medium size digital signal processing units, while it is very attractive from the analog design point of view.

Dušan P. Krčum – Department of Electronics, School of Electrical Engineering, University of Belgrade, Bulevar Kralja Aleksandra 73, 11020 Belgrade, Serbia; NovellC Microsystems, Veljka Dugoševića 54, Belgrade, Serbia, (e-mail: dusan.krsum@novelic.com).

Ivan M. Milosavljević – Department of Electronics, School of Electrical Engineering, University of Belgrade, Bulevar Kralja Aleksandra 73, 11020 Belgrade, Serbia; NovellC Microsystems, Veljka Dugoševića 54, Belgrade, Serbia (e-mail: ivan.milosavljevic@novelic.com).

Đorđe P. Glavonjić – Department of Electronics, School of Electrical Engineering, University of Belgrade, Bulevar Kralja Aleksandra 73, 11020

The paper is organized as follows. TIA specifications section describes main performance that TIA should achieve in typical digital audio broadcasting (DAB) environment. Detailed circuit design, including MPFB filter design approach, inverter core, and compensation network, is described in the TIA design section. Finally, simulation results of the designed TIA are shown in section IV.

II. TIA SPECIFICATIONS

TIA requirements for communication and optical systems generally may vary significantly. Consequently, it is difficult to design and implement circuitry that can be used for both systems. The main objective of this paper is to propose suitable TIA topology which can meet requirements of both systems. This paper describes TIA used in DAB systems, which are today widely popular in automotive industry.

Wide temperature range from -40 to 125 °C in automotive industry is among the most rigid requirement and introduces additional difficulties. Required TIA bandwidth can be obtained from the baseband receiver frequency in DAB systems. These frequencies are typically around 5 MHz. Another important specification is also related to channel width and spacing. Namely, due to crowded radio spectrum and scaling of technology which leads to lower supply voltages, design of radio receivers deal with large interferers and huge distortion of received signals. The most common parameters used for description of the distortion and linearity levels are third-order intermodulation product (IMD3) and input third-order interception point (IIP3). Exact values for these parameters depend on remaining circuits in the chain, but typical values can be derived from [1].

Area-efficient design is always desired in integrated circuits (ICs) to reduce overall cost, thus highlighting triple-inverter topology as the most suitable. On the other hand, automotive applications are among the most power hungry ones, thus proposed TIA design suffers from high current consumption. TIA requirements for DAB system are summarized in Table I.

III. TIA DESIGN

TIA topology is chosen based on the specifications given in Table I. Design of the MPFB filter and triple-inverter based amplifier is shown in this section.

Belgrade, Serbia; NovellC Microsystems, Veljka Dugoševića 54, Belgrade, Serbia (e-mail: djordje.glavonjic@novelic.com).

Darko M. Tasovac – Department of Electronics, School of Electrical Engineering, University of Belgrade, Bulevar Kralja Aleksandra 73, 11020 Belgrade, Serbia; NovellC Microsystems, Veljka Dugoševića 54, Belgrade, Serbia (e-mail: darko.tasovac@novelic.com).

Lazar V. Saranovac – Department of Electronics, School of Electrical Engineering, University of Belgrade, Bulevar Kralja Aleksandra 73, 11020 Belgrade, Serbia, (e-mail: laza@eff.bg.ac.rs).

TABLE I
TYPICAL TIA REQUIREMENTS FOR DAB RECEIVERS

Parameter	Value	Unit
Temperature range	-40 to 125	$^{\circ}\text{C}$
Bandwidth	5	MHz
Transimpedance Z_T	72	$\text{dB}\Omega$
Output referred noise	-25	$\frac{\mu\text{V}}{\sqrt{\text{Hz}}}$
IIP3	34	dBm
IMD3	-80	dBc

A. Multiple feedback filter design

Theory of MPFB filters is well known and is explained in great details in literature [2,3]. However, fast growing analog circuitry integration in many mixed-signal systems reveals new applications of MPFB filters. Among most popular is high dynamic range conditioning chains approaching ADCs.

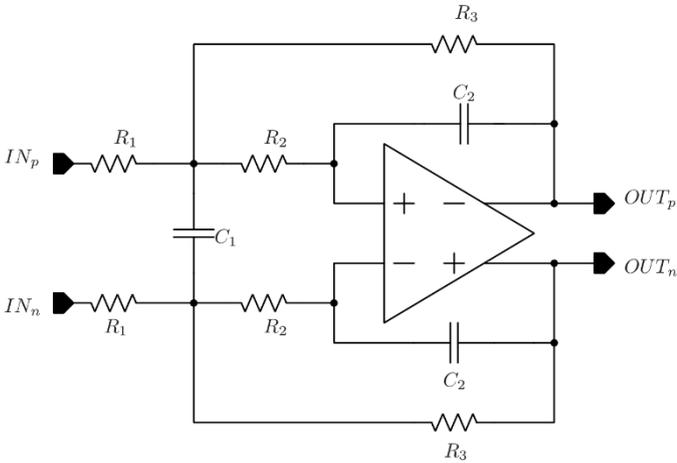


Fig. 1. Fully differential multiple feedback filter topology.

Transfer function of the MPFB filter shown in Fig. 1 is given as

$$H(s) = \frac{-\frac{1}{2C_1C_2R_1R_2}}{s^2 + s\left(\frac{1}{2R_1C_1} + \frac{1}{2R_2C_1} + \frac{1}{2R_3C_1}\right) + \frac{1}{2C_1C_2R_2R_3}}. \quad (1)$$

Low frequency gain is determined by ratio $-\frac{R_3}{R_1}$. Resistor R_3 is programmable in order to achieve programmable gain, and to be able to compensate process variations of the TIA. Resistor R_1 has typical value of few hundreds ohms for typical applications in integrated filters. It can be equivalent to the resistance of the switch in current mode mixer, and can be used instead of lumped component. Value of the capacitor C_1 dominantly determines position of the first pole, thus bandwidth trimming can be easily done by implementing this capacitor as capacitor bank.

B. CMOS inverter core

Amplifier within multiple feedback filter can be designed in various ways depending on top level specifications of the filter, primarily current consumption, noise, and distortion level. In Fig. 2 is shown fully differential topology of the amplifier based on triple-inverters as amplifying block.

Common mode signal is sensed using feedback network which is also designed using inverters.

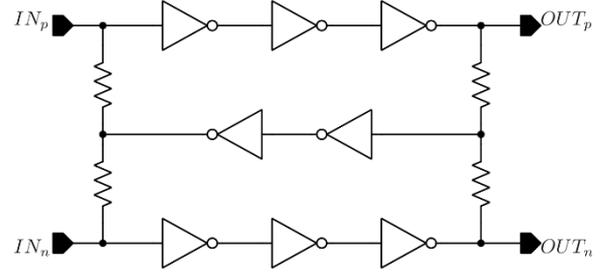


Fig. 2. Triple-inverter amplifier topology.

Inverters used in this implementation are custom made rather than standard digital cells due to many contradictory requirements. Optimization process of the triple-inverter topology is difficult, regardless of simplicity in terms of number of optimization parameters. One of the most challenging task in the design of this amplifier is to obtain stability over all process, voltage, temperature (PVT) variations, while keeping other design parameters within desired values. Combination of the nested and reversed nested Miller compensation network is implemented, which enables good compromise between bandwidth and distortion level [7]. Implemented compensation network is shown in Fig. 3. Compensation network ensures proper pole splitting and phase margin greater than 55° in all corners.

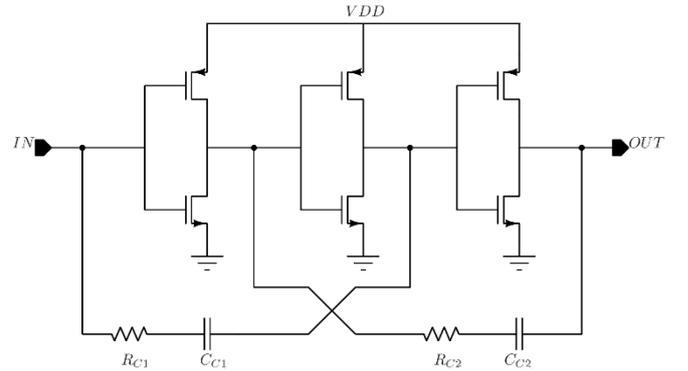


Fig. 3. Triple-inverter amplifier compensation network.

IV. SIMULATION RESULTS OF THE DESIGNED TIA

Designed TIA performance is characterized using Cadence© SpectreRF simulator with TSMC 65 nm technology.

In Fig. 4 transimpedance over frequency is shown. Typical in-band transimpedance is 72 $\text{dB}\Omega$, as required. 3-bit control word enables 8 gain steps with 2 dB spacing. Bandwidth can also be tuned from 2.5 MHz to 6 MHz, by using 3-bit control word to set proper value in the C_1 capacitor bank.

Noise performance in any analog integrated circuit is of great interest. Depending on the top level signal-to-noise ratio calculation, noise of each sub-circuit can be represented in various manners. Most common representation of the TIA noise is input referred current noise. However, output referred voltage noise can be used as figure of merit when succeeding blocks in chain are used for voltage processing, like in DAB systems.

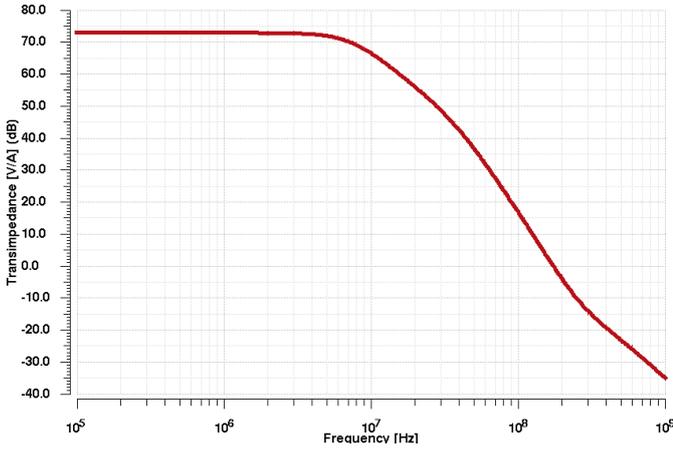


Fig. 4. Transimpedance of the TIA for different frequencies.

Output referred noise spectral density of the designed TIA is shown in Fig. 5.

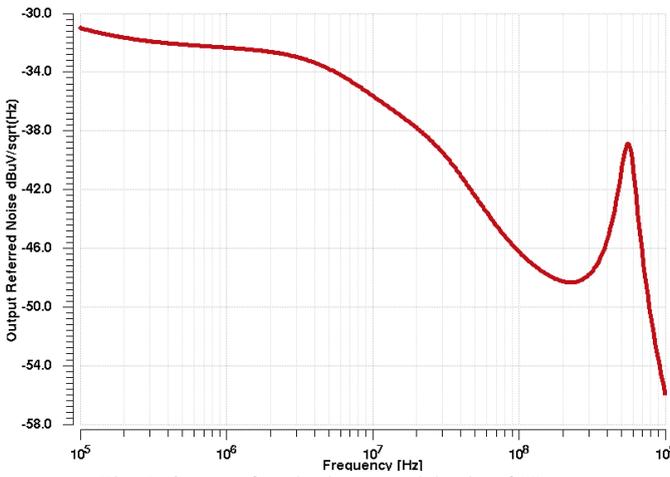


Fig. 5. Output referred noise spectral density of TIA.

In order to estimate distortion levels, two closely separated tones at 1 MHz and 1.8 MHz are applied at the TIA input. These tones are chosen as typical carriers in DAB baseband systems. Output spectrum is shown in Fig. 6. Third-order intermodulation product at 2.6 MHz is 84 dB under level of the input tone. Table II shows achieved performance of the designed TIA.

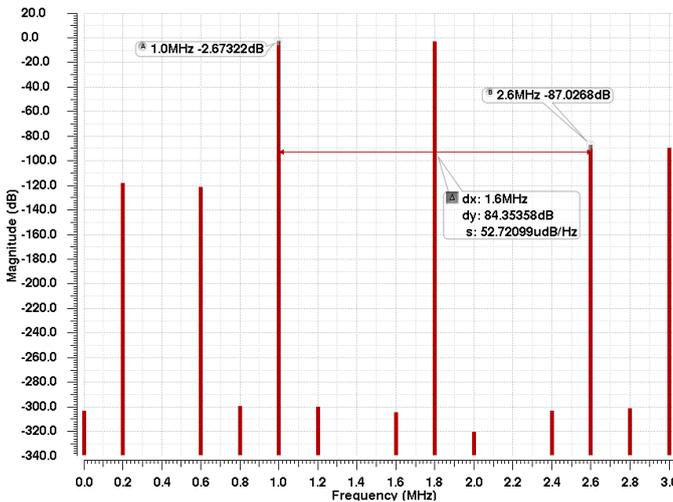


Fig. 6. Spectrum of the signal at the output of TIA for two close spaced input tones.

TABLE II
TIA PERFORMANCE COMPARISON

	Ref [5]	Ref [4]	Ref [6]	This work
Process	28 nm	180 nm	130 nm	65 nm
Power	5.4 mW	20.57 mW	1.92 mW	31.6 mW
BW	20 MHz	2.4 GHz	12 MHz	5 MHz
Z_T	-	72 dB Ω	80 dB Ω	72 dB Ω
Output referred noise	$-21.6 \frac{\mu\text{V}}{\sqrt{\text{Hz}}}$	$-37.2 \frac{\mu\text{V}}{\sqrt{\text{Hz}}}$	-	$-31 \frac{\mu\text{V}}{\sqrt{\text{Hz}}}$
IIP3	28 dBm	-	36 dBm	34 dBm
IMD3	-102 dBc	-	-70 dBc	-84 dBc

V. CONCLUSION

This work demonstrates the design and implementation of the transimpedance amplifier as a part of DAB receiver. TIA is implemented in standard 65 nm process. It has bandwidth of 5 MHz, IMD3 of -84 dBc, while consumes 31.6 mW. Achieved performance is comparable with the state-of-the-art designs found in literature. Simple CMOS inverters were used as amplifiers which saves area, but challenges stability of the amplifier. Crossing pole splitting compensation network between TIA stages is implemented while bandwidth, distortion level and noise performance were kept within desired margins. This design enables integration within radio or wired communication system, as well as within optoelectronics signal processing chains.

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