Multi-axis drive DC link current minimization

Luka Lopin, Nikola Lepojević

***Abstract*— Multi-axis drives increasingly attract the attention of the scientific community because of the benefits they provide in terms of price, compactness and energy-efficiency. This paper presents a method for reducing the effective current of DC link. The method is based on the optimal adjustment of phase difference of PWM carriers of each drive. Minimum effective current of DC link is obtained when phases of PWM carriers make arithmetic progression with step $180^0/n$, where n is number of drives in parallel. When drive changes over from motor mode to generator mode or vice versa, the minimum current of DC link is maintained by delaying its PWM carrier by 90^0.**

***Index Terms*— Multi-axis drive, Pulse width modulation (PWM), DC link current minimization, Phase-shifted carrier (PSC)**

I. INTRODUCTION

As compared to classical stand alone drive shown in Fig. 1, multi-axis drive systems are characterized by a common rectifier bridge and DC link to which multiple inverters are connected in parallel (Fig. 3). Common DC link enables power sharing between inverters, which significantly improves efficiency. It also contributes to savings in cost and improved compactness compared to more traditional stand alone drives [1]. Thus, proper design of DC link is important.

DC link in such systems usually consists of aluminum electrolytic capacitor [2] to:

- compensate instability of battery, or to filter non zero voltage harmonics on the output of rectifier bridge
- reduce the spreading of current harmonics with pulse frequency into the mains
- supply the input current of the inverter with pulse frequency
- ensure load's demands for transient power peaks

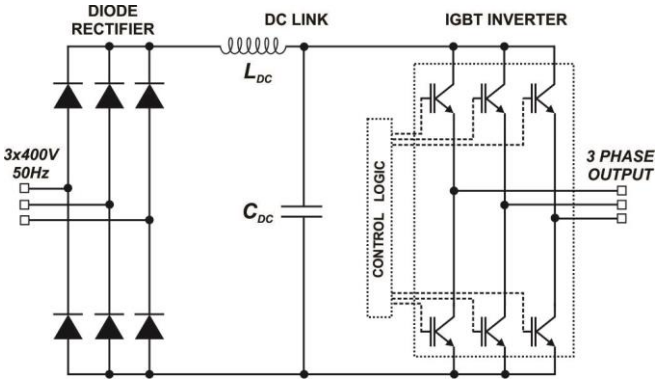

Fig. 1. Typical stand alone drive system

Working life of electrolytic capacitor depends on operating voltage and working temperature. When capacitor is operated at 0.9 rated voltage, the failure rate is lowered to 60% as compared to an operation at rated voltage. If the working temperature is lowered, the typical working life doubles for every 10^0 below the rated temperature [3], [4]. Therefore, in order to achieve the required mean time between failures (MTBF), in addition to proper selection of operating voltage, the correct thermal design is necessary.

A. Thermal design

Electrochemical processes occurs in the electrolytic capacitor. Its capacitance and equivalent series resistance are not stationary and depend on temperature and frequency [4], [5]. Temperature that influences the working life of the capacitor is capacitor can temperature. It is determined by ambient temperature and Joules losses in capacitor caused by its effective current (1) [2].

$$T_c = T_a + I_{c,rms}^2 R_{esr} R_{th,c-a} \tag{1}$$

- R_{esr} –equivalent series resistance of the capacitor which represents the sum of the frequency sensitive resistance of the oxide dielectric, the temperature sensitive resistance of the electrolyte and the relatively constant small contributions of the foil, the tabs and the terminals
- $R_{th,c-a}$ – heat transmission resistance between the capacitor can and the ambience
- T_c – capacitor can temperature
- T_a – ambient temperature
- $I_{c,rms}$ – DC link effective current

Thermal design is reduced to dimensioning DC link according to its effective current $I_{c,rms}$. Commonly, the effective current is calculated as the root mean square value of capacitor's current, shown in equation 2, where i_c is capacitor's current.

$$I_{c,rms} = \sqrt{\frac{1}{N}\sum_{n=o}^{N-1} i_c^2[n]} \tag{2}$$

- $i_c[n]$ – DC link current samples
- N – number of DC link current samples
- $I_{c,rms}$ – effective DC link current

B. Weighted effective current

Electrolytic capacitors are more persistent to high frequency currents [5]. For this reason, capacitor's effective current is weighted. However, a different approach then in eq. (2) is required weight effective current.

Luka Lopin is with the School of Electrical Engineering, University of Belgrade, 73 Bulevar kralja Aleksandra, 11020 Belgrade, Serbia (e-mail: lukalopin@yandex.com).

Nikola Lepojević is with the School of Electrical Engineering, University of Belgrade, 73 Bulevar kralja Aleksandra, 11020 Belgrade, Serbia (e-mail: nikola.lepojevic@etf.rs).

Capacitor's manufacturer provides frequency dependent coefficients for current weighting. These coefficients are listed in Table 1. Based on Yageo SK capacitor (6.3~100V, Below~68μF) [5] coefficients, part by part linear weighting curve is formed, shown in Fig. 2.

Frequency spectrum of capacitor's current is weighted by weighting curve. Using Parseval's theorem (3), one can seek weighted effective value of the current from the weighted spectrum [6].

$$\sum_{n=0}^{N-1} i_c^2[n] = \frac{1}{N}\sum_{k=0}^{N-1} I_c^2[k] \qquad (3)$$

TABLE I
COEFFICIENTS FOR CURRENT WEIGHTING

CURRENTS RIPPLE MULTIPLIER Frequency coefficient					
FREQ [Hz] / CAP [F]	120	300	1K	10K~100K	
6.3~100V Below~68μF	1.00		1.20	1.30	1.50
6.3~100V 100~680μF	1.00		1.10	1.15	1.20
6.3~100V 1000~22000μF	1.00		1.05	1.10	1.15
160~450V Below~220μF	1.00		1.25	1.40	1.40
160~450V Above~220μF	1.00		1.10	1.13	1.13

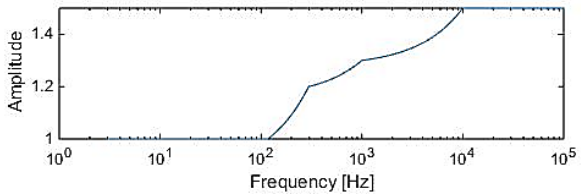

Fig. 2. Part by part linear weighting curve

II. MODEL AND SIMULATION

The aim of this paper is to examine the effects of phase-shifting PWM carriers of each drive on DC link effective weighted current. System modeling is based on two assumptions [7], [8].

- voltage of electrolytic capacitor is stable - capacitor is replaced with voltage source
- each inverter has ideally sinusoidal output current without ripple - load is replaced with current drain

Model is represented in Fig. 3. Three phase MOSFET inverters are loaded with three phase current drain. PWM block uses triangular carrier signal of frequency f_m. Its phase could be delayed by phase angle Φ_{mk}, $k\epsilon\{1,...,n\}$, where n is number of inverters in parallel. Index of modulation $M_k\epsilon[0,1]$ represents amplitude of three phase referent sinusoidal signal. By comparing triangular carrier and referent signal, six electrical signals are obtained for gating transistors.

Dead time is thirtieth part of period of PWM switching signal. It is possible to change power factor PF_k, by changing phase of current drain. When power factor was changed, corresponding index of modulation was also changed in order to obtain equal active power of all inverters. Models are formed with 2, 3, 4 and 5 inverters in parallel. All current drains have the same amplitude. DC link current is normalized relative to the peak value of the current drain. Then, the effects of phase-shifting PWM carriers of individual drives is examined on the normalized effective DC link current for the purpose of its minimization.

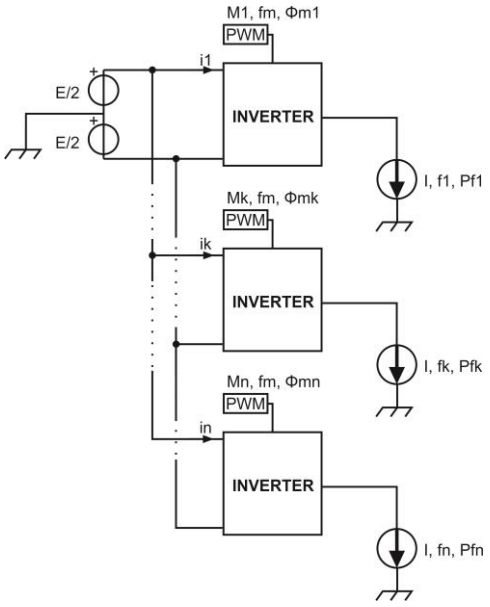

Fig. 3. Block diagram of the model

A. Two inverters in parallel

Inverter can operate in motor or generator mode. For the two inverters, there are four possible operation mode. Results of complementary modes are identical.

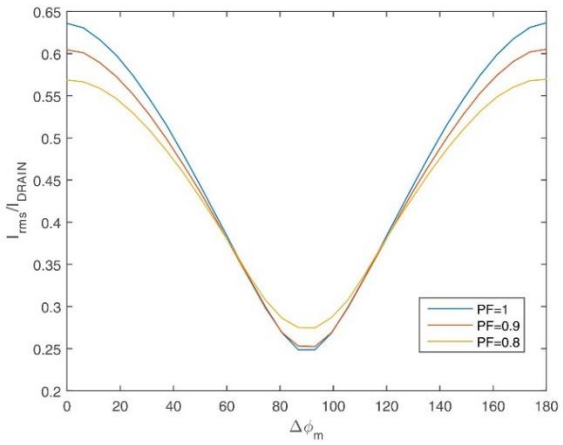

Fig. 4. Dependence of the DC link current and PWM phase difference of two inverters in parallel for various power factors. Both inverters are in same regime.

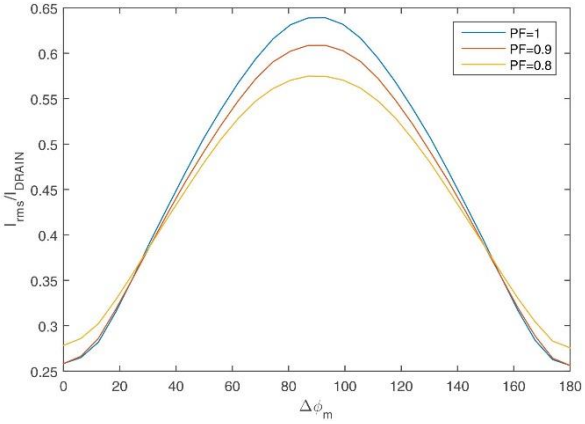

Fig. 5. Dependence of the DC link current and PWM phase difference of two inverters in parallel for various power factors. Inverters are in back to back mode.

When both inverters operate in same regime in Fig. 3, minimum current is obtained when phase difference is $\Delta\Phi_m=\Phi_{m2}-\Phi_{m1}=90^0$, where Φ_{m1}, Φ_{m2} are phases of PWM carriers of inverters 1, 2 respectively. When inverters operate back to back mode, as in Fig. 4, minimum current is obtained for $\Delta\Phi_m= \Phi_{m2}- \Phi_{m1}=0^0$.

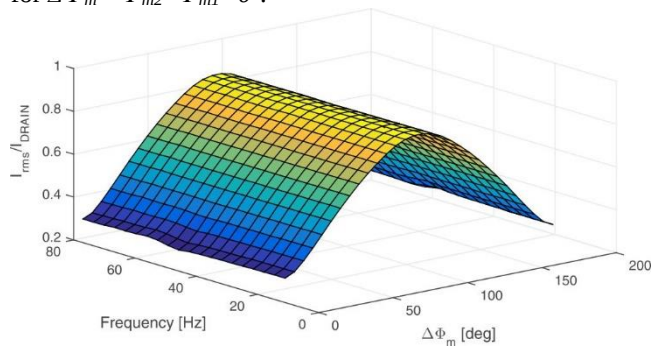

Fig. 6. Dependence of the DC link current, PWM phase difference of two inverters in parallel and frequency of inverter. Frequency of one inverter is fixed to 50 Hz. Frequency of other inverter has taken value from interval (10, 80) Hz.

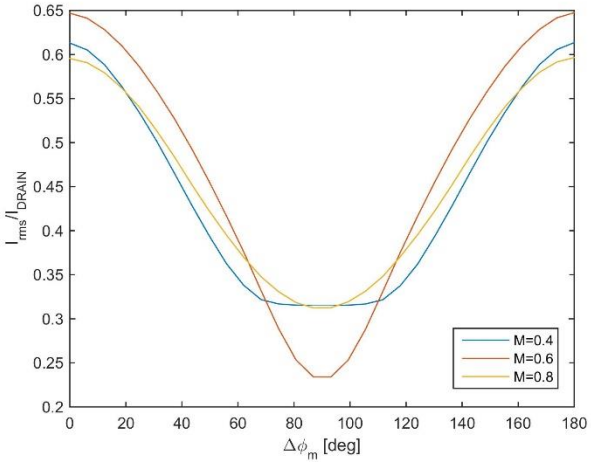

Fig. 7. Dependence of the DC link current and PWM phase difference of two inverters in parallel for various index of modulation.

Fig. 6 shows that frequency variation of the first inverter does not affect the effective current. Fig. 4, 5 show that power factor variation does not translate the curve along $\Delta\Phi_m$ axis, but it affects minimum and maximum values. Similar effect has variation of index of modulation as shown in Fig. 7.

B. Three inverters in parallel

For three inverters, there are eight different working regimes. Results of simulations of DC link effective current in function of $\Delta\Phi_{m1}$ and $\Delta\Phi_{m2}$ are shown in Fig. 8 – 11. Φ_{m1}, Φ_{m2}, Φ_{m3} are phases of PWM carriers of inverters 1, 2, 3 respectively and $\Delta\Phi_{m1}= \Phi_{m1}-\Phi_{m3}$, $\Delta\Phi_{m2}=\Phi_{m2}-\Phi_{m3}$, $\Phi_{m3}=0^0$. Value of minimum DC link current and its coordinates $\Delta\Phi_{m1}$ and $\Delta\Phi_{m2}$ are shown in Table 2. Working regimes on Fig. 8 – 11 match working regimes in Table 2. Complementary regimes have been omitted for the sake of clarity.

TABLE II
RESULTS OF CURRENT MINIMUM SEARCH

	P1	P2	P3	I_{rms}	$\Delta\Phi_{m1}[^0]$	$\Delta\Phi_{m2}[^0]$
1	0	0	0	0.3226	60º	120º
2	0	0	1	0.3225	150º	210º
3	0	1	0	0.3214	60º	210^0
4	0	1	1	0.3216	150º	120º
5	1	0	0	0.3216	150º	120º
6	1	0	1	0.3214	60º	210º
7	1	1	0	0.3225	150º	210º
8	1	1	1	0.3226	60º	120º
=0, mot. regime; =1, gen. regime				$\Delta\Phi_{m1}= \Phi_{m1}- \Phi_{m3}$; $\Delta\Phi_{m2}= \Phi_{m2}- \Phi_{m3}$; $\Phi_{m3}=0^o$		

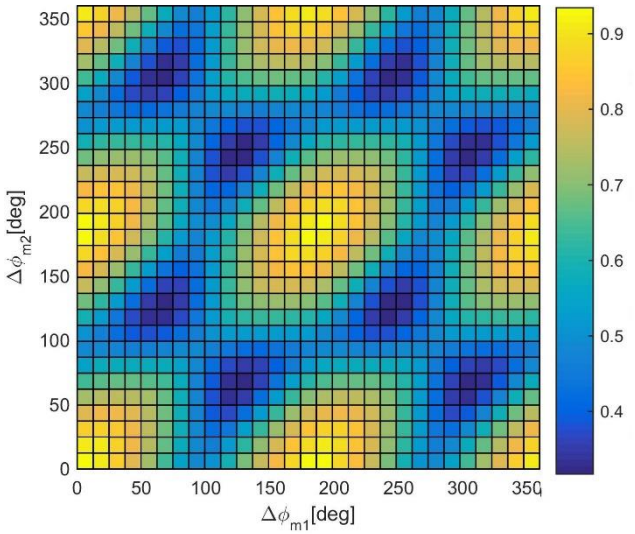

Fig. 8. Dependence of effective DC link current and PWM phase differences of the three inverters in parallel. Regime 000 and 111.

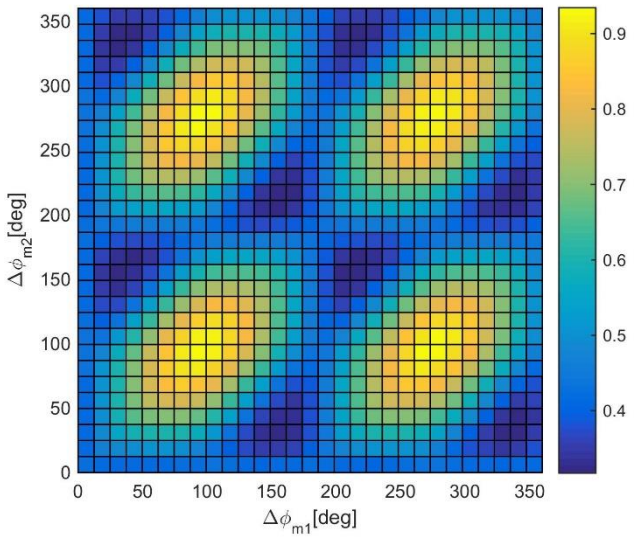

Fig. 9. Dependence of effective DC link current and PWM phase differences of the three inverters in parallel. Regime 001 and 110.

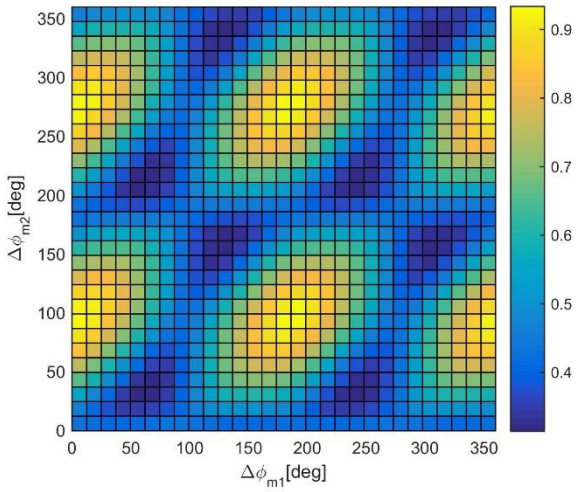

Fig. 10. Dependence of effective DC link current and PWM phase differences of the three inverters in parallel. Regime 010 and 101.

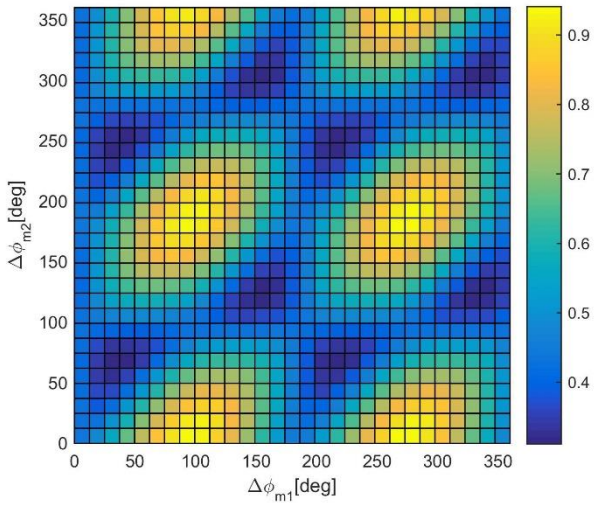

Fig. 11. Dependence of effective DC link current and PWM phase differences of the three inverters in parallel. Regime 011 and 100.

Periodicity of 180^0 along both axes can be observed in Fig. 8 – 11. For 000 or 111 regime current minimum is obtained for phases $[\Phi_{m3}\ \Phi_{m1}\ \Phi_{m2}] = [0^0\ 60^0\ 120^0]$, as shown in Fig. 8. For two inverters in parallel and regime 00 or 11 minimum current is obtained for phases $[\Phi_{m1}\ \Phi_{m2}] = [0^0\ 90^0]$, as shown in Fig. 4. Thus, minimum DC link current is obtained when phases of PWM carriers of each inverter make arithmetic progression with step $180^0/n$, where n is number of inverters in parallel.

For two inverters in parallel in Fig. 5, current minimum was shifted for 90^0 compared to Fig. 3 whether inverter 1 or 2 changed its regime. When operated with three inverters, 90^0 current minimum shifting along $\Delta\Phi_{m2}=\Phi_{m2}-\Phi_{m3}$ axis could be seen on Fig. 10 compared to Fig. 5 when inverter 2 changed its regime. Current minimum in Fig. 11 was shifted along $\Delta\Phi_{m1}=\Phi_{m1}-\Phi_{m3}$ axis for 90^0 compared to regime in Fig. 5 when inverter 1 changed its regime. Inverter 3 changed its regime in Fig. 9 compared to regime in Fig. 5 and DC link current minimum was shifted for 90^0 along both $\Delta\Phi_{m1}=\Phi_{m1}-\Phi_{m3}$ and $\Delta\Phi_{m2}=\Phi_{m2}-\Phi_{m3}$ axis. If inverter k, $k\epsilon\{1,\ldots,n\}$ changes over from motor to generator mode, or vice versa, minimum is maintained by adding 90^0 to phase Φ_{mk} of PWM carrier.

C. Four and five inverters in parallel

In this section four PWM carrier phase vectors were simulated for various working regimes for multi-axis drives with four and five inverters in parallel. 90^0 was added to PWM carrier phases of inverters in generator mode in the third and the fourth vector.

Table 3 and 4 presents the results of simulating the 4 and 5 inverters in parallel respectively. It is shown that minimum DC link current is obtained for the third and the fourth phase vector. Phases of PWM carriers in the fourth vector form arithmetic progression with step $180^0/n$. Because of periodicity of 180^0 it is possible to obtain minimal current with step $360^0/n$, if $n>2$.

TABLE III
FOUR INVERTERS IN PARALLEL

Regimes	$[\Phi_{m1}, \Phi_{m2}, \Phi_{m3}, \Phi_{m4}]$			
$[P_1\ P_2\ P_3\ P_4]$	[0º, 0º, 0º, 0º]	[0º, 180º, 0º, 180º]	[0º, 90º, 180º, 270º]	[0º, 45º, 90º, 135º]
0000	0.7242	0.7243	0.3597	0.2990
0001	0.6836	0.6843	0.3687	0.3268
0011	0.3857	0.3869	0.3689	0.3331
0111	0.6666	0.6616	0.3015	0.3376
P_i=0 - mot. regime; P_i=1 - gen. regime;				

TABLE IV
FIVE INVERTERS IN PARALLEL

Regimes	$[\Phi_{m1}, \Phi_{m2}, \Phi_{m3}, \Phi_{m4}, \Phi_{m5}]$			
$[P_1\ P_2\ P_3\ P_4\ P_5]$	[0º, 0º, 0º, 0º, 0º]	[0º, 180º, 0º, 180º, 0º]	[0º, 72º, 144º, 216º, 288º]	[0º, 36º, 72º, 108º, 144º]
00000	0.7300	0.7296	0.2000	0.1995
00001	0.7623	0.7629	0.3699	0.3691
00011	0.5185	0.5209	0.3670	0.3668
00111	0.5030	0.5031	0.3631	0.3619
01111	0.7090	0.7059	0.3049	0.3045
P_i=0 - mot. regime; P_i=1 - gen. regime;				

III. CONCLUSION

In this paper a simple method for minimization of effective DC link current of multi-axis drive system is proposed. This method doesn't require regulation. Implementation is simple and does not occupy significant computing resources. It is shown that the maximally effective DC link current could be reduced 50% by large, if the phases of PWM carriers of each drive make arithmetic progression with step $180^0/n$, where n is the number of drives on the DC link. Further, the minimum current can be sustained when drives change working regime if PWM carrier phase is delayed by 90^0 at the time of transition between working regimes. By halving DC link effective current, Joule's losses are decreased in DC link 4 times. Using this method MTBF of electrolytic capacitor is significantly prolonged, thus cost of maintenance of multi-axis drive is reduced.

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