BENEFITS OF MTR CONTRAINTS IN SOFT-OUTPUT DECODING OF LDPC – MTR CODES CONCATENATION OVER E^{2}PR4 CHANNEL MODEL

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Abstract – *Soft-output decoding and consequence of maximum transition run (MTR) constraints in low-density parity-check (LDPC) and MTR codes concatenation has been investigated. Iterative decoding of LDPC as an outer and MTR as an inner code in one-track one-head E^{2}PR4 magnetic recording channel is presented in proposed simulation scheme. Advantages have been confirmed with computer simulation results.*

1. INTRODUCTION

Growing need for storing massive amount of data extends areal recording densities in hard-disc drives. Increasing linear recording density by reducing lengths of magnetic domains along the track, results in nonlinear distortions of magnetization and thermal instability of domains. Those phenomenons manifests through increased intersymbol interference (ISI).

In order to maintain channel linearity and to reduce ISI level, a certain minimum distance is maintained between successive transitions in magnetization of elementary domains. Minimum distance is accomplished by imposing restrictions on sequences of transitions, such that certain error-patterns are avoided [1]. This method helps channel detector to make better estimations and thus practical recording systems should employ certain type of constrained coding. As a solution, a maximum transition run (MTR) codes can be considered [2].

Mainly, MTR codes have been developed to enhance distance properties at the channel output. By preventing ±[+1 –1 +1] error-event in high-density magnetic recording systems, such as E^{2}PR4 and ME^{2}PR4 channel model, these codes facilitate achievement of channel matched-filter-bound (MFB) and therefore increase channel minimum squared-Euclidean distance [3]. Furthermore, MTR codes ability to reduce number of channel trellis states and effortless hardware realization enlarge possibility of their employment as integral part of magnetic recording systems. This fact has motivated many researchers for further improvements of MTR codes capabilities [4], [5].

Recently, low-density parity-check (LDPC) [6], and MTR codes concatenation attracted attention in magnetic recording systems. Todd and Cruz presented idea which imposes MTR constraints in decoding of LDPC code over partial response magnetic recording channels [7]. MTR code has been used as an outer and LDPC as an inner code in proposed simulation scheme, providing gain about 0.2dB.

Unfortunately, configuration like those one could not utilize MTR ability for channel trellis states reduction, preserving overall decoding complexity high. Also, decoding process of MTR codes, based on hard decision, turns into limiting factor for full utilizations in soft-output decoding. In order to employ MTR codes in soft-output and consequently in iterative decoding scheme, propagation of soft information trough MTR coder/decoder has to be accomplished [8].

Soft-output coding/decoding of MTR codes and their implementation in iterative decoding process is analysed, in this paper. Log-likelihood ratio (LLR) algebra utilisation in Boolean logic functions and consequences to iterative decoding is presented in Section II. LDPC – MTR code concatenation in iterative decoding scheme is considered in Section III, while computer simulation results are presented in Section IV. Finally, concluding remarks are given in Section V.

2. LLR ALGEBRA UTILISATION IN MTR CODES

MTR codes are designed to eliminate ±[+1 –1 +1] error-event [1]. Consequence of this constraints leads to exclusion of 1010 and 0101 patterns from channel input sequences, and to channel trellis reduction from 16 to 14 states, as depicted in Fig. 1.

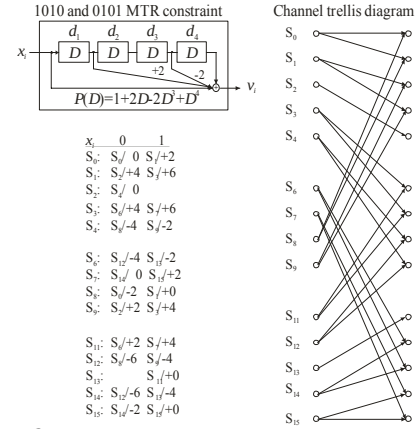

Fig. 1 *E^{2}PR4 channel trellis with MTR constraints*

MTR fulfills fast coding/decoding process requirements, because simple and low-cost hardware implementation can be done using logic circuits, as shown in Fig. 2.

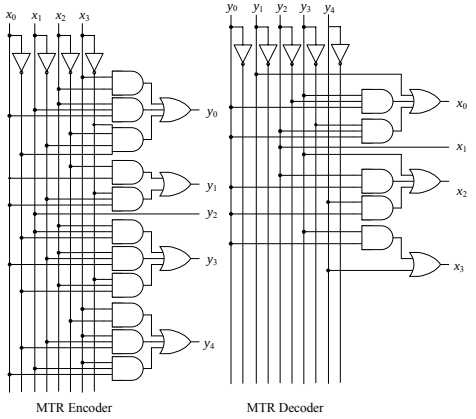

Fig. 2 *Rate 4/5 (k_1 = 2, 8) MTR encoder/decoder hardware implementation*

Circuit optimization task was not considered here.

Iterative decoding process, where LDPC acts as outer and MTR as inner code, involves propagation of soft-output information through coders/decoders. MTR codes are based on

Boolean logic circuits so propagation requires log-likelihood ratio (LLR) algebra implementation in those circuits [8].

Using LLR for binary variable x:

$$LLR(x) = \log \frac{P(x=0)}{P(x=1)}, \tag{1}$$

easily can be shown that LLR for Boolean NOT logic output can be expressed as

$$LLR(\bar{x}) = -LLR(x), \tag{2}$$

where logarithm is natural logarithm. In this way soft information easily propagates through Boolean NOT circuits.

LLR approach also can be applied for Boolean AND logic output as

$$LLR(x_1 \text{ AND } x_2) = \log(e^{LLR(x_1)} + e^{LLR(x_2)} + e^{LLL(x_1)+LLR(x_2)}), \tag{3}$$

where statistical independency of binary variables x_1 and x_2 is assumed. Hardware realization of *log*() and *exp*() operations in digital systems is not so easy task and their straightforward implementation can not yield simple and fast decoding process. Fallowing approximation

$$LLR_{app}(x_1 \text{ AND } x_2) = \max[LLR(x_1), LLR(x_2)], \tag{4}$$

simplify hardware realization of LLR algebra implementation in Boolean AND logic circuits. Approximation (4) in certain degree accompany the exact expression, while largest deviation appears when LLR of Boolean AND operands increases, as shown in Fig. 3.

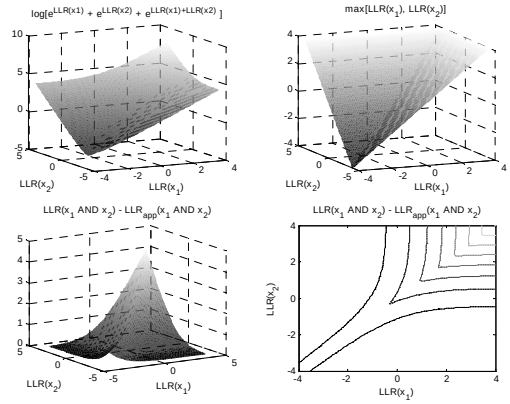

Fig. 3 LLR of Boolean AND logic and its approximation

Disagreement is not so critical problem because in moments when it appears Boolean AND logic circuit result, obtained by exact expression and approximation, is known with similar high reliability which is enough for proper estimation. Therefore, the exact reliability is not highly important.

Employing LLR algebra for Boolean OR logic output the fallowing expression is obtained

$$LLR(x_1 \text{ OR } x_2) = -\log(e^{-LLR(x_1)} + e^{-LLR(x_2)} + e^{-(LLL(x_1)+LLR(x_2))}), \tag{5}$$

where statistical independency of binary variables x_1 and x_2 is assumed, also. Simple hardware realization is possible using fallowing approximation

$$LLR_{app}(x_1 \text{ OR } x_2) = \min[LLR(x_1), LLR(x_2)]. \tag{6}$$

In this case deviation of LLR approximation from the exact expression (5) is shown in Fig. 4.

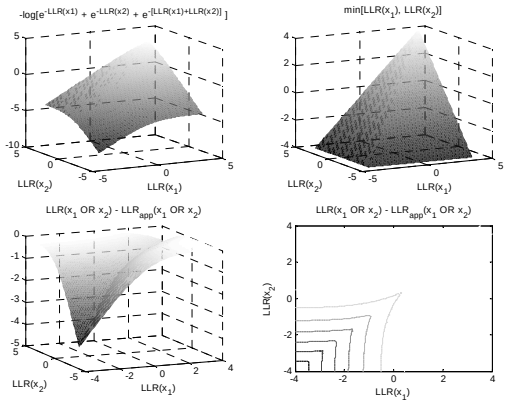

Fig. 4 Boolean OR logic LLR and its approximation

It can be noticed that largest disagreement appears when LLR of both Boolean OR operand decreases, but in that case the results of Boolean OR logic is already known with high reliability, also.

Finally, LLR of Boolean XOR logic output can be represented as

$$LLR(x_1 \text{ XOR } x_2) = \log \frac{1 + e^{LLR(x_1)} e^{LLR(x_2)}}{e^{LLR(x_1)} + e^{LLR(x_2)}}, \tag{7}$$

assuming statistical independency between x_1 and x_2. Using fallowing approximation

$$LLL(x_1 \text{ XOR } x_2) = sign[LLR(x_1)] \cdot sign[LLR(x_2)] \cdot \min[LLR(x_1), LLR(x_2)], \tag{8}$$

simple and fast hardware propagation of soft-output information is possible. Deviation of approximation is show in Fig. 5.

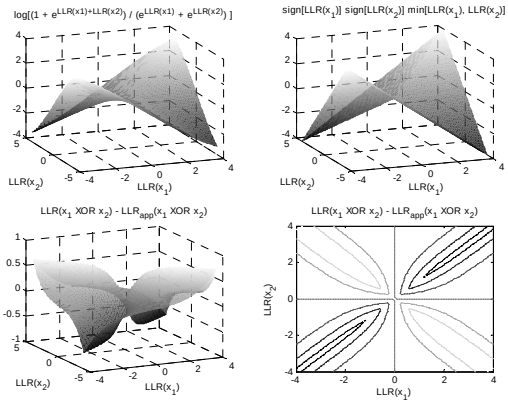

Fig. 5 LLR of Boolean XOR logic and its approximation

Small degree of deviation appears when XOR operands have similar LLR value, but because logic result is known in those moments, exact reliability is not highly important.

The LLR algebra implementation in Boolean logics enable spreading of soft-output information, simplifying hardware realization of MTR soft-output coding/decoding process and its iterative decoding utilization.

3. LDPC – MTR CODES CONCATENATION

LDPC – MTR codes concatenation was performed using rate 4/5 (k_1 = 2, 8) MTR as inner and rate R = 0.96 LDPC as outer code. The LDPC of length N = 4732 with M = 169 parity bits, and with column-weight 3, is based on Kirkman triple systems [9]. Overall code rate of LDPC - MTR concatenation is R = 0.768.

The coding process of LDPC – MTR concatenation was simulated in one-track one-head magnetic recording system targeted to E^2PR4 partial response model, as depicted in Fig. 6.

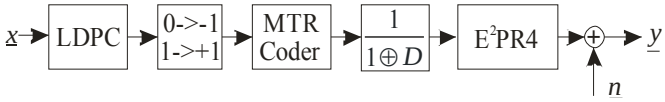

Fig. 6 LDPC – MTR coding over E^2PR4 channel

It was assumed that read back signal ***y*** is distorted with additive, white and zero-mean, Gaussian noise ***n*** and that signal-to-noise ratio (SNR) is defined as

$$SNR = 10\log\left(\frac{E_b}{N_o}\right) = 10\log\left(\frac{E_c}{2R\sigma^2}\right), \qquad (9)$$

where $E_c=RE_b$ is symbol bit energy at channel output, N_o is one-sided power spectral density and σ^2 is noise variance.

Channel output sequence detection is performed with optimum soft-output Viterbi detector (SOVA), with 20 symbols detection window while LDPC decoding by message-passing algorithm [13]. Assuming that y_i is noisy received symbol and that x_i is noiseless trellis transition label the branch distance was calculated as

$$(y_i - x_i)^2 + u_i \cdot LLR_i^{MESS.PASS.}, \qquad (10)$$

where u_i is trellis information bit label at time instant i.

Decoding of LDPC – MTR codes concatenation where soft-output information was exchanged between decoders is considered for two cases.

Case A) SOVA – message-passing forwarding

In this case during decoding process soft-output information was transmitted from SOVA to message-passing algorithm, only, as depicted in Fig. 7.

There is no return path between message-passing and SOVA, so soft-output information exchanges in one direction only. This simulation case can not be considered as iterative decoding process but its analysis is valuable in situation when overall decoding complexity reduction is important.

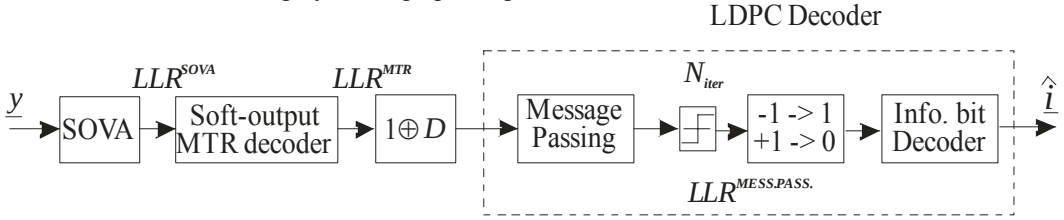

Fig. 7 SOVA – message-passing soft-output information forwarding

Case B) SOVA – message-passing – SOVA exchange

In this case during decoding process soft information exchanges between SOVA and message-passing, through MTR soft-output coder, as depicted in Fig. 8.

Soft-output information from message-passing referred as $LLR^{MESS.PASS.}$, is delivered back to the SOVA detector in order to help him to calculate trellis branch distance and to try to improve channel sequence estimation from previous iteration.

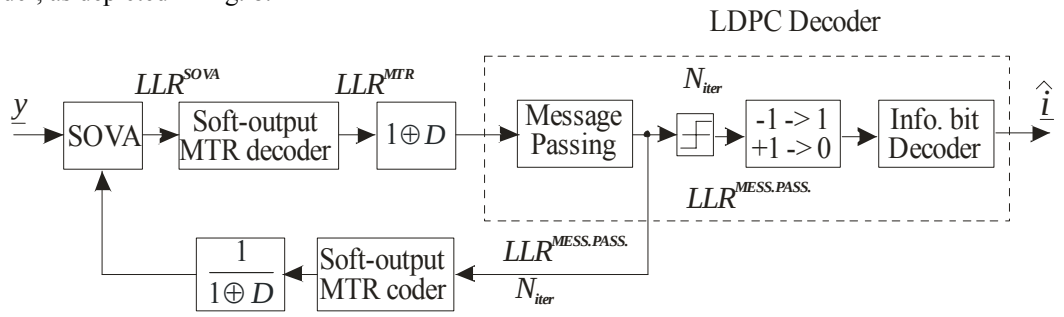

Fig. 8 SOVA – message-passing – SOVA soft-output information exchange

4. SIMULATION RESULTS

Possible increasing of overall decoding complexity when iterative decoding process is utilized encourages analyses of soft-output MTR decoding in *Case A*), shown in Fig. 7. In proposed scheme the simple forwarding of soft-output information is present while SOVA detection process is alleviate.

Preserving MTR constraints the channel detection trellis complexity is reduced for about 12%, because the number of trellis states is decreased from 16 to 14. This can be useful in circumstances where channel trellis complexity presents limiting factor for effortless and fast channel sequence detection [11], [12].

In this case decision of LDPC codeword bits was based on message-passing soft output information $LLR^{MESS.PASS.}$, and simulation results are depicted in Fig. 9.

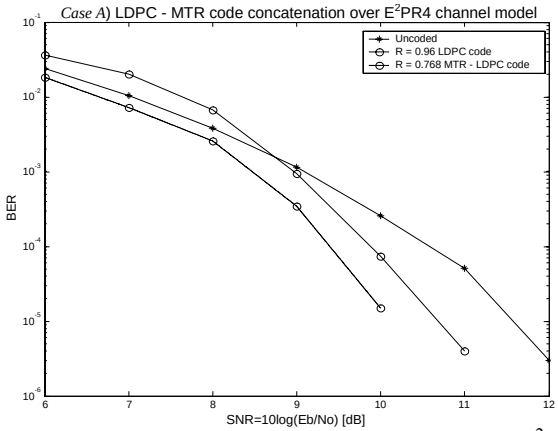

Fig. 9 *Case A*) R = 0.768 LDPC – MTR code over E^2PR4 channel

As a consequence of MTR code implementation in proposed concatenation the overall code rate is decreased. Using LDPC – MTR code with lower code rate then single LDPC, gain of 0.6dB for BER = 10^{-5} is obtained, indicating possible usefulness of LDPC – MTR codes concatenation. Moreover, R = 0.768 LDPC – MTR code has resulted in 1.7dB coding gain for BER = 10^{-5} compared with uncoded case.

The second simulation scenario considers behavior of the soft-output MTR coder/decoder in an iterative decoding case. The idea was to check the overall performance and decoding complexity of proposed iterative decoding scheme, in situation when SOVA detector receives message-passing soft information to improve channel sequence detection. Simulation has been performed with N_{iter} = 5 iterations.

Unfortunently, MTR coder output codeword bit, as can be seen from Fig. 2, is

$$x_0 = y_1 + y_0\bar{y}_2y_3 + y_0y_2\bar{y}_3, \qquad (11)$$

and its LLR is highly conditioned with LLR of several input bits. It means that soft-output information, which propagates through soft-output MTR coder in return path, becomes statistically dependent. Consequently, when the number of iteration is increased statistical independency in (4), (6) and (8) can not be exactly assumed. Therefore, utilization of soft-output MTR coder produces poorer iterative decoding results compared with first scenario case, as shown in Fig. 10.

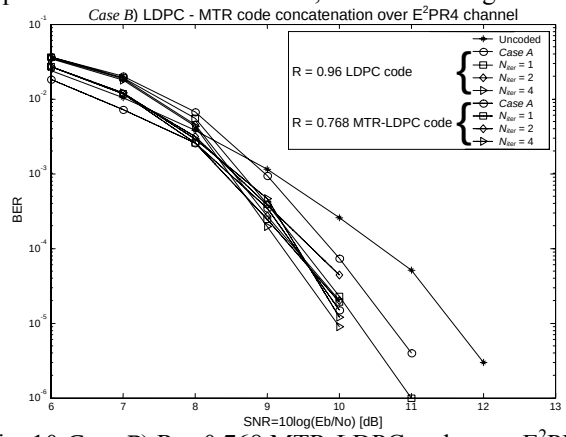

Fig. 10 *Case B*) R = 0.768 MTR-LDPC code over E^{2}PR4 with increased number of iterations

Obtained results with no extra coding gain are not so unexpected. High dependencies are present in soft-output MTR coder/decoder codeword bits, resulting with less reliable soft-output information. Such unreliable information can not help SOVA detector to improve its decisions.

However, analysis of LLR algebra implementation have shown that fast and effective propagation of soft-output information through MTR coder's/decoder's logic can be done. Obtained simulation results are not worst than the case when only R = 0.96 LDPC code is present.

5. CONCLUSION

In this paper soft-output coding/decoding of MTR codes was analyzed. It is shown that fast and effective propagation of soft-output information can be obtained utilizing LLR algebra in MTR Boolean logic circuits. Using MTR as an inner and LDPC as an outer code in an iterative decoding scheme over E^{2}PR4 model, the overall decoding complexity has been decreased, since reduction of number of channel trellis states from 16 to 14 is present.

Ignoring increased decoding complexity in iterative decoding scenario, simulation results shows that increased number of iteration resulted with no extra coding gain compared with result for first iteration. But, notice that R = 0.768 LDPC – MTR codes concatenation has a 1.7dB coding gain for BER = 10^{-5} compared with uncoded case.

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Sadržaj: U ovom radu analizirano je soft-output dekodovanje kao i posledice maximum transition run (MTR) ograničenja u rednoj vezi low-density parity-check (LDPC) i MTR kodova. Iterativno dekodovanje LDPC, kao spoljašnjeg, i MTR, kao unutrašnjeg koda, razmatrano je na E^{2}PR4 kanalu za magnetski zapis sa jednom stazom i jednom glavom za čitanje.