CURRENT DIFFERENCING CMOS VOLTAGE-CONTROLLED TRANSCONDUCTOR AND RESISTOR

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Abstract - *The presented CMOS voltage-controlled transconductor and floating resistor are based on the current difference of two nonsaturated MOSFETs with equal source-to-drain voltages. A new type of the summing-differencing current circuit is introduced. The circuits operate at a supply of ± 1.5 V. Simulations show nonlinearities below 1.4 % for input voltage swings up to ± 0.5 V, and 5 % frequency bandwidths above 70 MHz.*

1. INTRODUCTION

Voltage-controlled transconductor (VCT) [1] and voltage-controlled resistor (VCR) [2] employ the current difference of two nonsaturated MOSFETs with equal drain-to-source voltages. Two source-coupled pairs degenerated by nonsaturated MOSFETs are used. Transconductances (resistances) are independent of the MOSFETs' threshold voltages. Their values can be varied by the difference of two control voltages over a wide range without affecting the input voltage range. They are insensitive to substrate noise and to noise common to the control voltages. Both the positive and the negative transconductances (resistances) can be obtained. However, the designs [1] and [2] are based on the assumption that the gate-to-source voltages of the input source-followers carrying different currents are equal. They can be made only nearly equal in the case of large *W*/*L* ratios of the MOSFETs used. This is the main source of the linearity errors in [1] and [2]. Another VCT and floating VCR CMOS architecture suitable for low-voltage operation using current differencing principle and avoiding considered drawback is presented in this paper. A novel type of summing-differencing current circuit (SDCC) is also introduced and used as a building block of both the VCT and the VCR.

2. CIRCUIT DESCRIPTION

The drain currents of the matched nonsaturated p-channel MOSFETs M_1 and M_2 with common substrate [3] are given by

$$I_{Di} = \beta_{pi}\left[\left(V_{SGi}+V_{tpi}\right)V_{SDi} - \frac{1}{2}\left(1+\frac{\partial V_{tpi}}{\partial V_{BSi}}\right)V_{SDi}^2\right] \qquad (1)$$

where variables have their usual meanings, and i=1, 2, with $\beta_{p1}=\beta_{p2}=\beta_p$. If their source and drain voltages are equal, then the threshold voltages are also equal $V_{tp1}=V_{tp2}$, and the current difference is

$$I_{D1} - I_{D2} = \beta_p\left(V_{G2}-V_{G1}\right)V_{SD}\,. \qquad (2)$$

Providing the equality of the source-to-drain voltages $V_{SD1}=V_{SD2}=V_{SD}$ and the input voltage V_{IN} of the transconductor (resistor), (2) can be used to design a controllable transconductor (resistor). The block diagrams of the proposed VCT and floating VCR are shown in Figs. 1*a*) and 1*b*), respectively. Two SDCCs, two matched p-channel MOSFETs M_1 and M_2 with the common substrate, and two control voltages V_{C1} and V_{C2} are used in the proposed approach.

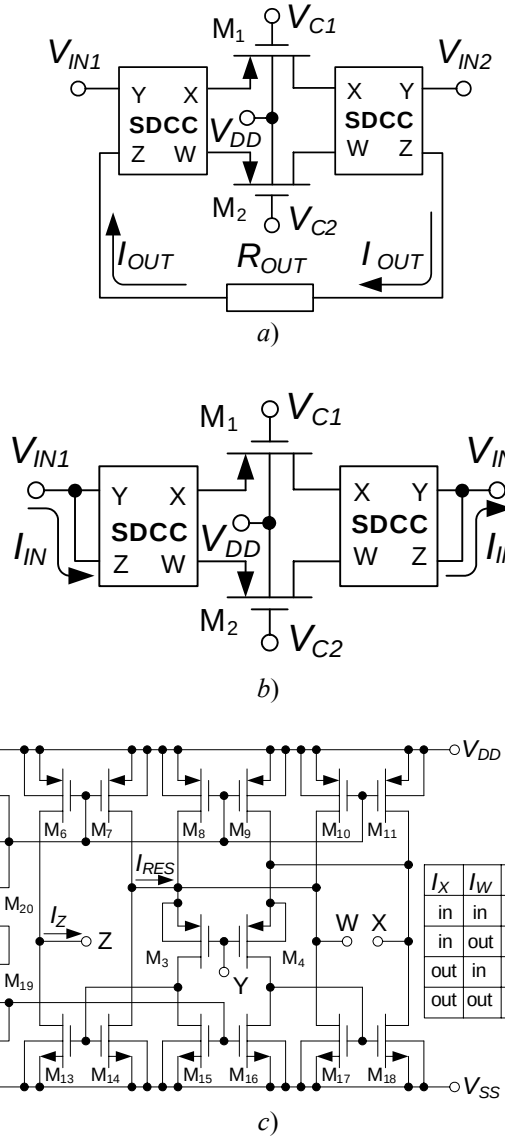


Fig. 1 *Proposed voltage-controlled transconductor and floating resistor*
a) Block diagram of the voltage-controlled transconductor,
b) Block diagram of the voltage-controlled resistor,
c) Summing-differencing current circuit.

A new type of SDCC is shown in Fig. 1*c*). The output current flowing through the node Z is equal to the sum or to the difference of the currents flowing through the nodes X and W. The equality of the voltages at the nodes X and W is realized by the source followers M_3 and M_4 carrying the equal and constant currents $I_{D3}=I_{D15}=I_{D16}=I_{D4}=const$. Because no body effect occurs in M_3 and M_4, their source-to-gate voltages are equal and constant $V_{SG3}=V_{SG4}=const$. The signs "+" and "-"in the table shown in Fig. 1*c* depend on the directions of the currents I_X and I_W. For example, the following equalities are valid for the first case ("in-in"): $I_{D8}=I_{D9}$, $I_{D10}=I_{D11}$, $I_{D17}=I_{D18}$, $I_{D17}=I_W+I_{D10}+I_{D8}-I_{D3}+I_{RES}$ and $I_{D18}=I_X+I_{D11}+I_{D9}-I_{D4}$. Hence, the resulting current entering the node W is $I_{RES}=I_X-I_W$. The current follower M_6-M_7-M_{13}-M_{14} with $I_{D6}=I_{D7}$ and $I_{D13}=I_{D14}$ is involved to transfer the current I_{RES} toward the node Z. The currents $I_{D6}=I_{D7}$, $I_{D8}=I_{D9}$, $I_{D10}=I_{D11}$, and $I_{D15}=I_{D16}$ are determined by the bias current formed by M_5, M_{12}, M_{19}, and M_{20}.

Taking into account (2) and Fig.1, the output current of the VCT (the input current of the floating VCR) is derived as

$$I_Z = I_{RES} = I_X - I_W = I_{D1} - I_{D2} = \beta_p \left(V_{C2} - V_{C1}\right) V_{IN} \qquad (3)$$

where $V_{IN}=V_{IN1}-V_{IN2}=V_{SD1}=V_{SD2}=V_{SD}$. The transconductance G_m and the resistance R_{EQ} of the proposed VCT and floating VCR, respectively, can be written as

$$G_m = \frac{1}{R_{EQ}} = \beta_p \left(V_{C2} - V_{C1}\right). \qquad (4)$$

Linearity is not affected by the body effect in M_1 and M_2 because it occurs in an equal measure for both devices and cancels out. Assuming the simple quadratic model of the saturated M_3 and M_4, the control voltage ranges can be found to be $V_{C1} < \min\{V_{IN1}, V_{IN2}\} + (2I_{D4}/\beta_{p4})^{1/2}+V_{tp1}-V_{tp4}$ and $V_{C2} < \min\{V_{IN1}, V_{IN2}\} + (2I_{D3}/\beta_{p3})^{1/2}+V_{tp2}-V_{tp3}$, with $V_{tp1}=V_{tp2}$, $V_{tp3}=V_{tp4}$, $I_{D3}=I_{D4}$, and $\beta_{p3}=\beta_{p4}$.

3. SIMULATION RESULTS

The operation of VCT and floating VCR shown in Fig. 1 has been simulated using SPICE with a level 3 MOS transistor model for AMIS ABN n-well CMOS process with 1.5 μm feature size (λ=0.8 μm) obtained by MOSIS. The *W*/*L* dimensions of the MOSFETs used are the following (in μm/μm): 6.4/1.6 (M_1, M_2), 8/1.6 (M_{12}, M_{13}, M_{14}), 11.2/1.6 (M_{15}, M_{16}), 16/1.6 (M_5, M_8, M_9), 24/1.6 (M_{17}, M_{18}), 184/1.6 (M_3, M_4), 200/1.6 (M_6, M_7), 240/1.6 (M_{19}, M_{20}), and 336/1.6 (M_{10}, M11). Resistor R_{OUT}=12 kΩ, control voltage V_{C2}=-1.5 V, and supply voltages of ± 1.5 V have been used.

DC transfer characteristics of VCT for different values of the control voltage V_{C1} are shown in Fig. 2. One of the inputs has been grounded, V_{IN2}=0. The input voltage $V_{IN}=V_{IN1}$ has been swept from -0.5 V to 0.5 V. The worst-case linearity error is lower than 1.4 %, except for V_{C1}=-1.5 V, when it increases at the end of the input voltage range. DC transfer characteristics of VCR with the same values for V_{C1}, V_{C2}, and V_{IN} are similar to those shown in Fig.2.

The frequency characteristics of VCT and VCR for

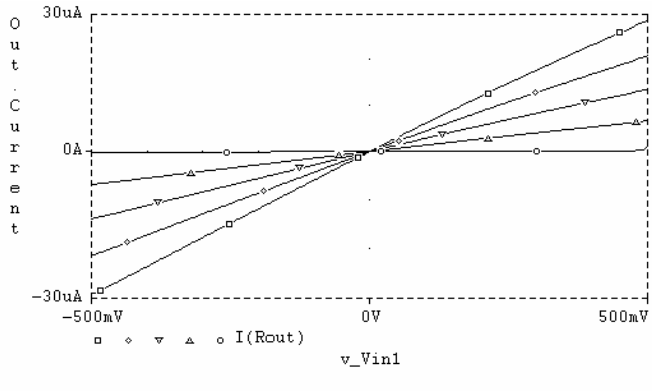
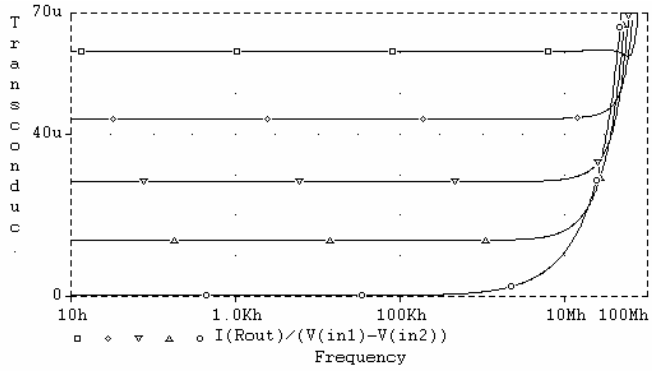
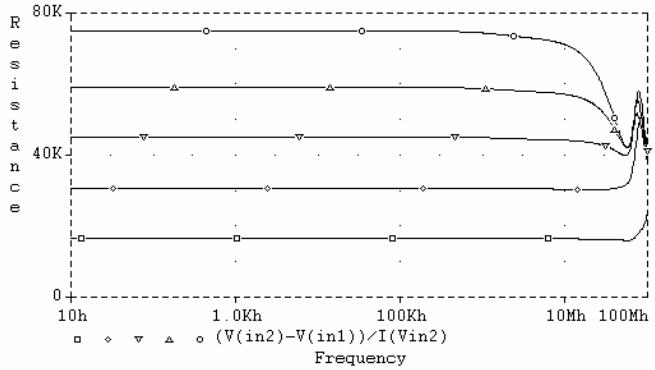


Fig.2: *Output current versus input voltage of the transconductor* (V_{C2}=-1.5 V)
□ V_{C1}=-0.4 V,
◇ V_{C1}=-0.675,
▽ V_{C1}=-0.95 V,
△ V_{C1}=-1.225 V,
○ V_{C1}=-1.5 V.



a)



b)

Fig. 3 *Frequency characteristics of the transconductor a) and the resistor b*) (V_{C2}=-1.5 V)
□ *a*) V_{C1}=-0.4 V, *b*) V_{C1}=-0.4 V
◇ *a*) V_{C1}=-0.675 V, *b*) V_{C1}=-0.87 V
▽ *a*) V_{C1}=-0.95 V, *b*) V_{C1}=-1.06 V
△ *a*) V_{C1}=-1.225 V, *b*) V_{C1}=-1.16 V
○ *a*) V_{C1}=-1.5 V, *b*) V_{C1}=-1.23 V

different values of V_{C1} are shown in Figs. 3*a* and 3*b*, respectively. The ± 5 % frequency bandwidth of the transconductance is 70.5 MHz for V_{C1}=-0.4 V (G_m=60.4 μS).

The ± 5 % frequency bandwidths of the shown resistances are larger than 10 MHz, and is 74 MHz for V_{CI}=-0.4 V (R_{EQ}=16.6 kΩ). Finally, the total power consumption for both VCT and VCR is 1mW.

4. CONCLUSION

A voltage-controlled CMOS transconductor and floating resistor based on current difference of two nonsaturated MOSFETs with equal source-to-drain voltages have been discussed. The transconductance (resistance) can be both positive and negative, and independent of the devices' threshold voltages. They show good bandwidth and linearity, and a ± 1.5 V operation.

REFERENCES

[1] Y. Tsividis, Z. Czarnul, and S. C. Fang, "MOS transconductors and integrators with high linearity", *Electronics Letters*, vol. 22, pp. 245-246, 27th Feb. 1986.

[2] K. Nagaraj, "New CMOS floating voltage-controlled resistor", *Electronics Letters*, vol. 22, pp. 667-668, 5th June 1986.

[3] Y. Tsividis, *Operating and modeling of the MOS transistor*, 2nd edition, New York: McGraw-Hill, 1999.

Sadržaj – Predstavljeni naponom kontrolisan CMOS transkonduktor i otpornik baziraju se na razlici struja dva MOSFET-a u omskoj oblasti rada sa jednakim naponima sors-drejn. Upotrijebljen je novi tip kola za realizaciju operacija sabiranja i oduzimanja u strujnom domenu. Napon napajanja kolâ je ± 1.5 V. Simulacije ukazuju na nelinearnosti manje od 1.4 % za promjene ulaznog napona do ± 0.5 V, i frekventni opseg iznad 70 MHz, koji je definisan kao odstupanje od ± 5 % u odnosu na transkonduktanse i otpornosti pri jednosmjernim pobudama.

NAPONOM KONTROLISAN CMOS TRANSKONDUKTOR I OTPORNIK NA BAZI RAZLIKE STRUJA

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