

FAULT EFFECTS IN SIGMA-DELTA MODULATOR

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Abstract - In this paper the fault effects in sigma-delta modulator are examined. The output signals of the fault-free and of the faulty circuits are transformed using the Fast Fourier Transformation. The influence of both hard and soft faults is captured, while this information can be very useful in the circuit diagnosis.

1. INTRODUCTION

Every complex system is liable to faults or failures. In most general terms a fault is any change in a system that prevents it from operating in the proper manner. We define diagnosis as the task of identifying the cause of a fault that is manifested by some observed behavior. Then some method of determining what fault has occurred is required. This is most often considered to be a two-stage process: firstly the fact that fault has occurred must be recognized – what is referred to as fault detection. Secondly, the nature should be determined such that appropriate remedial action may be initiated.

The explosion of integrated circuit technology has brought with it some difficult testing problems. The recent growth of mixed analogue and digital circuits complicates the testing problem even further. It becomes more complicated to determine a set of input test signals and output measurements that will provide a high degree of fault coverage. There is also a timing problem of testing the circuits even on the fastest automated equipment.

In this paper we will try to map the faults in the sigma-delta modulator to the Fast Fourier Transformation (FFT) of the output signal. Sigma-delta modulator is chosen as an example of the complicated mixed-signal circuit. It contains analogue, as well as digital elements, and what is more important, sigma-delta modulators are tolerant to circuit non-idealities and component mismatch. It means that faults are not easy to detect. Only single faults are considered.

2. SIGMA-DELTA MODULATOR ARCHITECTURE

Sigma-delta modulators are very attractive for design low frequency high-resolution analog-to-digital converters. Sigma-delta modulators trade speed for resolution. They employ coarse quantization in one or more feedback loops. By sampling at a frequency that is much greater than the signal bandwidth, it is possible for the feedback loops to shape the quantization noise so that most of the noise power is shifted out of the signal band. The out of band noise can then be attenuated with a digital filter. The degree to which the quantization noise can be attenuated depends on the order of the noise shaping and the oversampling ratio [1].

In addition to their tolerance for circuit nonidealities, oversampled A/D converters simplify system integration by

reducing the burden on the supporting analog circuitry. Because they sample the analog input signal at well above the Nyquist rate, precision sample-and-hold circuitry is unnecessary. Also, the burden of analog antialiasing filter is considerably reduced. Much of its function is transferred to the digital decimation filter, which can be designed and manufactured to precise specifications, including a linear phase characteristic.

3. CONCEPTS OF DIAGNOSIS

Besides the human expert that is usually performing the diagnostic project, one needs tools that will help, and what is most desired, will perform diagnosis automatically. Such tools are a great challenge to design engineers that pertains to the fact that generally the diagnostic problem is indeterminate. In addition, it is a deductive process with one set of data creating, in general, unlimited number of hypotheses among which one should try to find the solution. This is why permanent attention of the research community is attracted by this problem [2].

During the life-cycle of a product, testing is implemented in both the production phase and the implementation phase. We claim, however, that the sustainability of a product is strongly influenced by the design phase. So, to make a sustainable product, one should design the test procedure and synthesize test signals early in the design phase.

It is frequently possible to perform functional verification of the system. That, most frequently, happens when a small number of input/output terminals is present. In the majority of cases however, full functional testing becomes time consuming and is not acceptable. So, one applies defect-oriented (structural) testing, as will be discussed in more detail as follows.

We consider testing to be: the selection of a set of defects regarded as the most probable, the description of a set of measurements, the selection of a set testing points (or output signals) and most importantly, the synthesis of optimal testing signals that will be applied at the system inputs allowing for detectability and observability of the listed fault effects. Here, optimality means that one test signal covers as many faults as possible.

Selection of the type of measurements and testing points is specific to the circuit. One should stick to those measurements that are prescribed for functional verification. Specific measurements such as supply current monitoring are frequently adopted, too. Separate test points may be added in order to improve detectability or observability. Specific design for testability concepts can be applied.

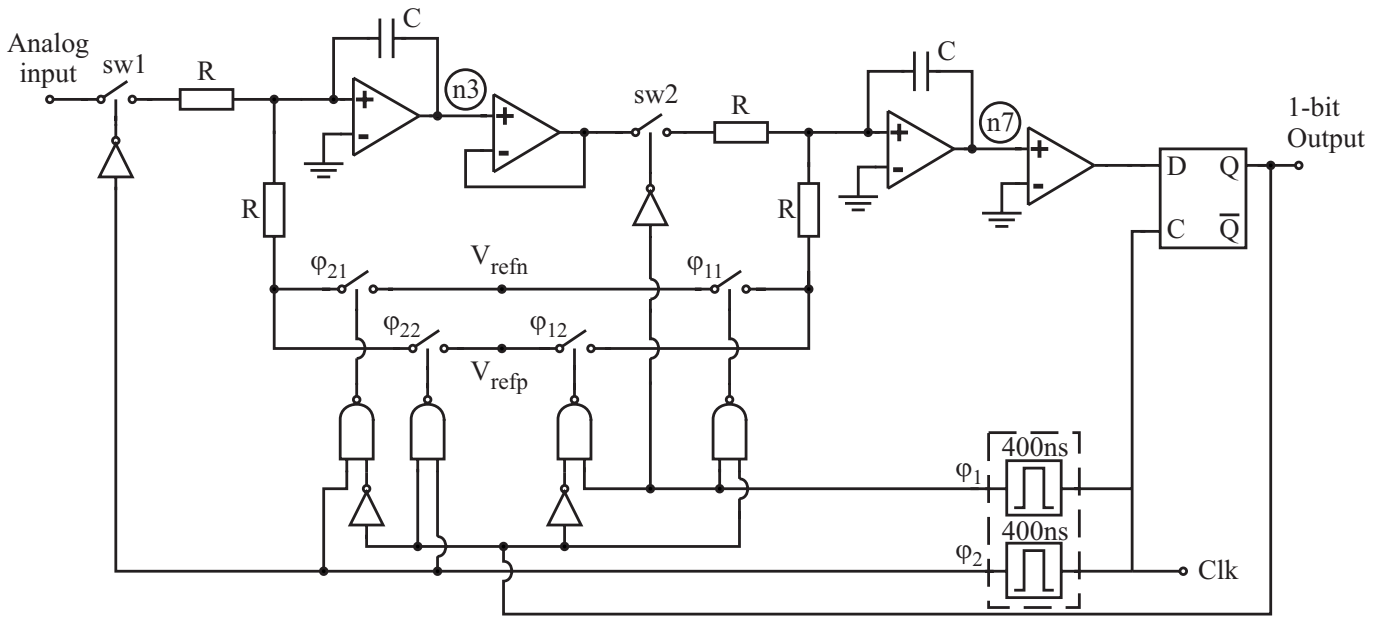


Fig. 1. Sigma-delta modulator architecture

After selection of test signals, the fault coverage has to be evaluated. To do that, as many replicas of the original circuit as the number of predicted faults have to be created. For large complex systems containing mechanical, analogue and digital parts, the number of replicas becomes huge. Each replica has one fault inserted. The fault coverage is evaluated after simulation of the faulty systems by comparing the results thus obtained with the response of the fault-free system. To reduce the computational effort, algorithms have been proposed to simulate multiple faulty circuits concurrently in both the analogue and the digital domains but not in mixed signal, and mixed description systems.

4. FAULTS IN THE SPECIFIC MODULATOR DESIGN

As an example of a complex circuit, the sigma-delta modulator in Fig. 1 is chosen [3].

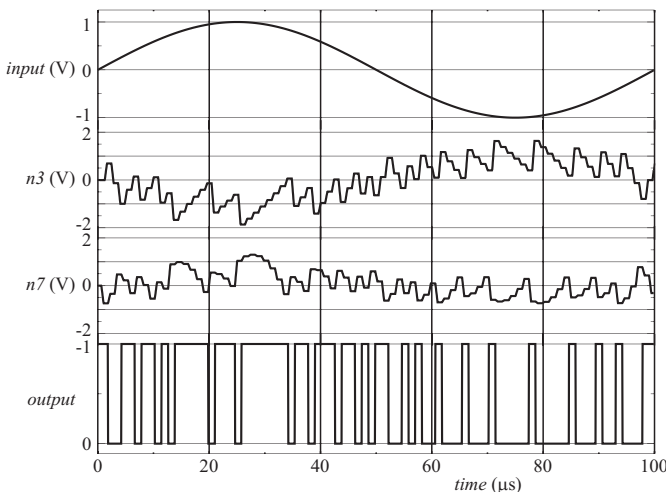


Fig. 2. Simulation results for linear sinusoidal excitation

This is a mixed-signal circuit, having both analogue and digital elements. Switches in the circuit are modeled as truly ideal switches, with zero resistance for closed switch and infinite resistance for open switch.

The integrator charging time is invariable with respect to clock rate in order to keep the gain constant. This means that the analog switch must be turned on for fixed time duration regardless of clock rate. This is achieved by using monostable multivibrator as a fixed-width pulse generator in the circuit. The monostable multivibrator between the clock input and switch control block functions as a pulse generator to produce control signals of fixed time duration. Fig. 2 shows reaction of the system when the input is excited by a sinusoidal signal.

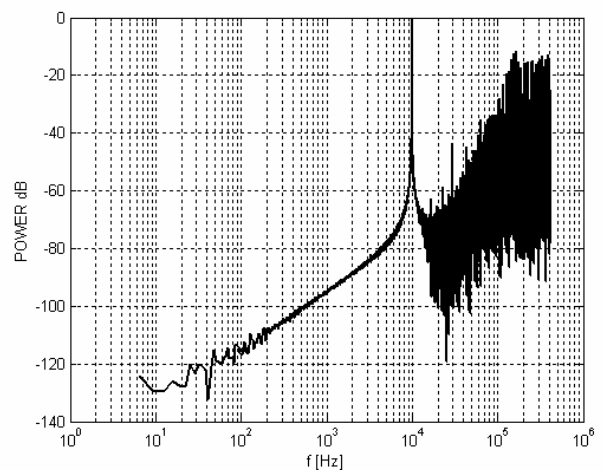


Fig. 3. FFT of the fault-free circuit

Simulations are performed using Alecsis [4] simulator. Transient response of a circuit of such complexity is impossible to analyze. Therefore, in order to detect faults,

output signal spectrum is observed. To obtain sufficient data for FFT, 256k samples are needed.

We applied 2V_{pp}, 10kHz sinusoidal signal to the modulator input. Clock frequency, f_s is 833.33kHz. Operational amplifiers are ideal with 10^5 gain and maximal output voltage level is clamped to $\pm 12V$. Circuit elements are: $R=1k\Omega$, $C=800pF$.

Power spectrum of the fault-free modulator output is presented in Fig. 3. It is seen from figure that the carrier frequency is 10kHz, and the noise floor increases at 40dB/dec. The architecture realizes a second-order noise shaping.

Presented spectra are normalized to the maximum spectral component.

The cases when switches in the feedback loop (ϕ_{11} , ϕ_{12} , ϕ_{21} , ϕ_{22}) are permanently closed are excluded, because voltage references V_{refp} and V_{refn} would be shorted.

There exist two groups of faults in every circuit: hard (catastrophic) faults, and soft (parametric) faults.

5. HARD FAULTS

Hard faults refer to an analogue circuit, and they change the circuit topology. In the circuit in Fig. 1, hard faults are modeled as switches that are stuck at ON, or stuck at OFF state. Modeling faults in digital circuits is much simpler. Digital signal can be “stuck-at-1” or “stuck-at-0”. In the circuit in Fig. 1, analogue switches are controlled by digital signals, so there are pairs of the same fault effects, such as: the effect is the same when the switch is stuck at ON (OFF) and the digital circuit is “stuck-at-1” (“stuck-at-0”). So, we will consider hard faults as stuck switches.

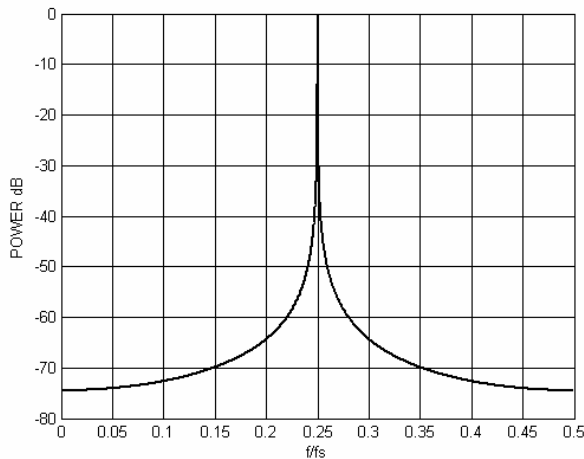


Fig. 4. FFT of the circuit output when switch $sw1$ is stuck at OFF

In Fig. 4., FFT of the circuit output when switch $sw1$ is stuck at OFF is shown. The switch $sw1$ is connected to the circuit input, so, when it is OFF, there is no input signal to the circuit. Output has no carrier, only clock subharmonic at $f_s/4$.

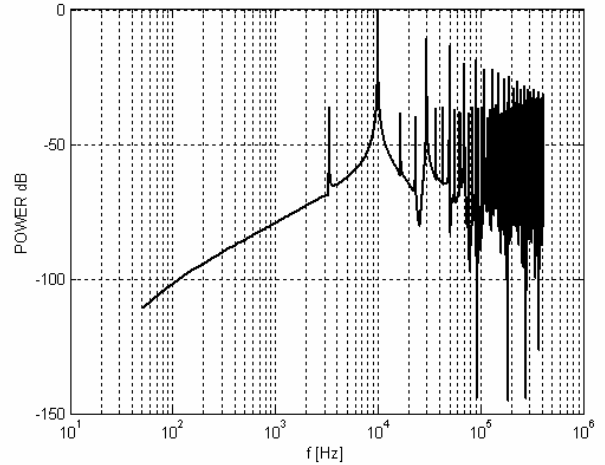


Fig. 5. FFT of the circuit output when switch $sw1$ is stuck at ON

Fig. 5 gives output spectrum of the circuit when switch $sw1$ is stuck at ON. First modulator stage behaves as the continuous integrator, therefore periodically overloads. Carrier is decreased due to saturation, and tone idles can be noted.

In Fig. 6, we have situation that switch ϕ_{11} is stuck at OFF. The V_{refn} voltage is disconnected and the ability to track input voltage is reduced. Integrator goes to overload which in turn decreases SNDR (Signal to Noise Distortion Ratio) as can be seen from Fig 6.

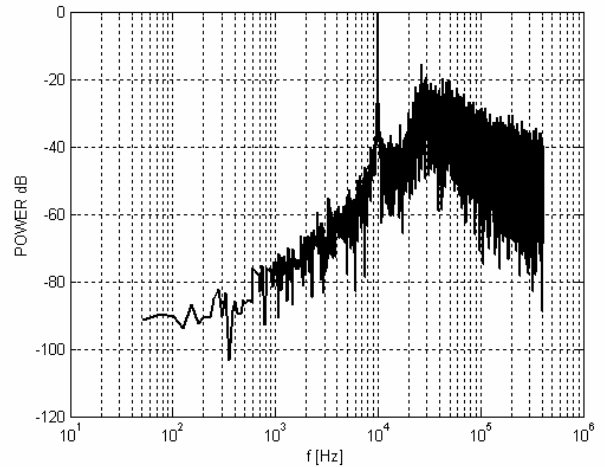


Fig. 6. FFT of the circuit output when switch ϕ_{11} is stuck at OFF

6. SOFT FAULTS

Soft (parametric) faults occur in the circuit when the value of some parameter is changed. The influence of soft faults to the frequency characteristics of the circuit can sometimes be catastrophic. In fact, change of the certain parameter can cause an unacceptable change in boundary frequency of the circuit or the system, so the circuit or the system can become unusable, although the topology has not changed [5].

Sigma-delta modulator is a very robust circuit, inherently tolerant to variations in circuit parameters, so fault effects are more difficult to be recognized.

We considered variations of the operational amplifier gain and capacitor values. First stage is more sensitive to parameter variations, while the changes in the second stage have minimum effect on the performance, due to noise shaping.

In Fig. 7 FFT of the circuit output when the gain of the first operational amplifier is decreased from 10^5 to 100. Small DC gain can cause integrator leakage to the low frequencies. The influence of this change is not quite observable. Change in FFT is too small to be usable.

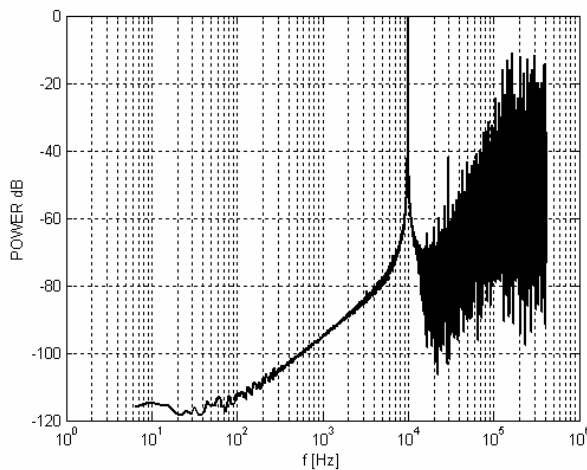


Fig. 7. FFT of the circuit output when the gain of the first operational amplifier is decreased to 100

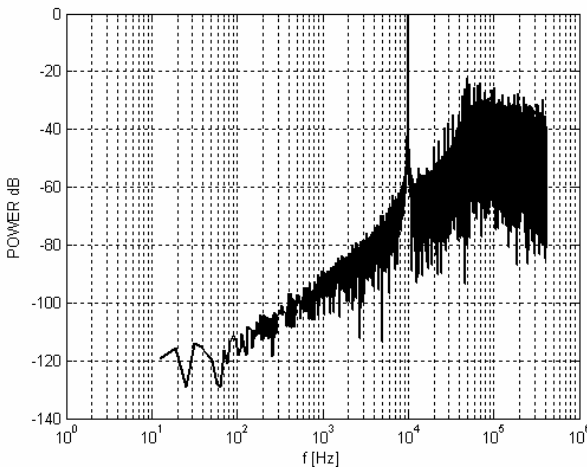


Fig. 8. FFT of the circuit output when the value of C is decreased 60%

Change of the capacitance values in the circuit can also influence its output. In this paper, the value of the capacitor in the first stage is changed. Decreasing the capacitance will increase integrator's output voltage, causing saturation. This leads to SNDR decrease, as shown in Fig. 8.

7. CONCLUSION

Fault effects in sigma-delta modulator were examined. The output signals of the fault-free and of the faulty circuits were transformed using the Fast Fourier Transformation. The influence of both hard and soft faults is captured, while this information can be very useful in the circuit diagnosis. We found this approach easy to implement for testing and diagnosis, since it requires simple testing equipment, no additional circuitry and only one testing point.

REFERENCES

- [1] Candy, J., Temes, G.: "Oversampling methods for A/D and D/A conversion", in *Oversampling Delta-Sigma Data Converters*. New York: IEEE Press, 1992, pp. 1-29.
- [2] Bandler, J., and Salama, A., "Fault diagnosis of analog circuits", *Proceedings of the IEEE*, Vol. 73, No. 8, August 1985, pp. 1279-1325.
- [3] Xu, X., and Lucas, M. S. P.: "Variable-Sampling-Rate Sigma-Delta Modulator for Instrumentation and Measurement", *IEEE Transactions on Instrumentation and Measurement*, Vol. 44, No. 5, October 1995, pp. 929-932.
- [4] Glozić, D., "Alecsis 2.1: An object-oriented hybrid simulator", Ph.D. thesis, University of Niš, Serbia, 1994, (in Serbian).
- [5] Litovski V. B.: "Projektovanje elektronskih kola: simulacija, optimizacija, testiranje, fizičko projektovanje", *Nova Jugoslavija, Vranje*, 2000.

Sadržaj – U radu su predstavljeni efekti defekata u sigma-delta modulatoru. Izlazni signal ispravnog kola, a zatim i kola sa defektom su transformisani Brzom Furijeovom Transformacijom. Prikazan je uticaj i tvrdih i mekih defekata, zato što ti podaci mogu biti veoma korisni u dijagnostici kola.

EFEKTI DEFEKATA U SIGMA-DELTA MODULATORU

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