Development of Testing Environment for a Discrete D/A Converter Using NI High-Speed M Series Acquisition Device

Anđela Jovanović, Miljana Milić and Marko Dimitrijević

Abstract – **A testing environment for the D/A converter board is suggested in this paper. The system required hardware-software co-design. It is intended for the demonstration purposes at the Course of Electronic circuit testing and diagnostics and enables students to study effects of different types of defects that could appear in one mixed-signal circuit. Necessary testing signals are applied from the computer, via the acquisition device to the inputs of the converter, and obtained voltage levels at the output of the D/A converter are measured and recorded for further analyses. The software part is realized using LabVIEW programming tool.**

Index Terms – **D/A converter, acquisition device, LabVIEW.**

I. Introduction

A digital-to-analog converter (DAC) is an integrated or a discrete circuit that converts a digital number into an appropriate value of voltage or current [1]. DACs are used to control devices that require a range of voltages or currents such as electro-acoustic transducers (speakers), some types of variable-speed motors, and many other applications. A widespread usage of DACs is for waveforms creation from digital signals – for example in CD players [2].

In the first years of testing, numerical values obtained from different instruments were handwritten on a paper, in order to analyze the results off-line. The paper was the easiest medium for a real-time display of measured signals. Advances in technology, eventually, enabled the tape recording of measurements' results in the form of continuous chart using a pen. By the end of the 1980s paper-based and magnetic tapes and charts were the most popular recording methods for the scientific data [3].

In the early 1960s, before the appearance of the first personal computer (PC), the IBM company has introduced computers that were particularly developed for scientific data recordings. This was enabled by IBM 7700 Data Acquisition System as well as the later IBM 1800 Data Acquisition and Control System [4]. These systems were very expensive and massive and required significant programming and organization to perform well. However, they were all forerunners of today's PC-based data acquisition systems.

Further advances in this field were made in the mid-1980s, when the National Instruments Corporation released to the market some data acquisition cards and analog-to-digital converter boards (DAQ board) that could be combined with a low-cost personal computer [4]. Beside the application of a PC as a data acquisition platform, the most important software program that enabled programming and functioning of such systems was LabVIEW, released in 1986 for Macintosh personal computers [5]. The LabVIEW enabled engineers to program in a graphical environment and develop their specific DAQ system. LabVIEW also offered many built-in functions necessary for data processing, data analysis and data display in real-time on the computer's monitor. In 1992 National Instruments released a version of LabVIEW for graphical operating systems such as Microsoft Windows and that compatibility is still maintained.

Scientists and engineers use data acquisition systems in their laboratory research, industrial control, test and measurement. A data acquisition and control system typically consist of the followings:

- Sensors, which measure physical variables such as temperature, strain, pressure, flow, force and motion (displacement, velocity and acceleration).
- Signal conditioning part, that converts the sensor outputs into signals readable by the analog input board (A/D) in the PC.
- An analog input (ADC) board, to convert these signals into digital format usable by the PC.
- A computer with the appropriate application software to process, analyze and log the data to disk. Such software may also provide a graphical display of the data.
- An output interface, to provide an appropriate process control response.

In this paper, we will suggest a specific testing environment i.e. acquisition system for performing different tests of the digital-to-analog converter, that uses a specific NI High-Speed M Series Acquisition Device [6]. The paper is organized as follows. The following section gives a short overview of the testing methods that apply to DACS. After that, a testing hardware will be suggested and described. A corresponding software part of the testing environment will be explained next. The paper ends with the interpretation of the testing results, followed by the concluding remarks.

II. Testing of the DAC

DC performance test is the first test that should be applied when verifying the functionality of the DAC [7]. The test checks for a steady linear response. A DC performance test setup is shown in Fig. 1. The signal source generates a ramp that performs voltage level and timing signal conditioning,

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and such ramp is delivered to the digital pin. A voltage ramp is generated at the DAC analog output by applying the corresponding sequential digital vectors. The output voltage is then digitized in order to enable efficient analysis of the response using the test system's Digital Signal Processor (DSP). The DSP subtracts the digitized DAC output from a calculated ideal value, and the obtained difference can be used to evaluate the DAC's DC performance.

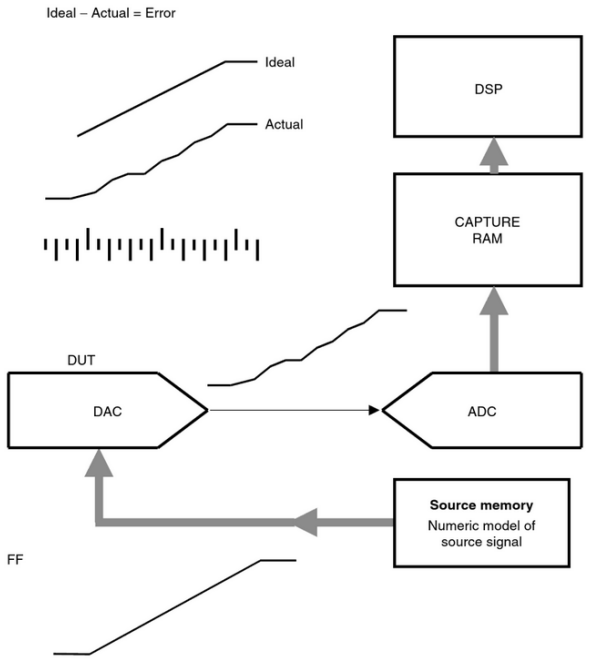

Fig. 1. A basic test setup for testing the DC performance of a DAC

The DAC's resolution can be defined as the number of different output voltage levels that it produces [7]. For example, a DAC with a resolution of 12 bits will be capable of producing 2^{12} or 4,096 different voltage levels at its output, while the DAC with a 16 bits resolution can generate 2^{16} or 65,536 different levels at its output. The resolution of the test system must overperform the resolution of the device under test when testing the accuracy of each DAC output voltage.

There are two general categories of DC tests for DAC devices [7]. The first category evaluates the device minimum and maximum output levels, referenced to an absolute specification. The offset is defined as the minimal output level, while the gain is defined in relation to the overall output signal span - from the minimum to the maximum. The second category of DC tests evaluates the device linearity, according to a relative step size value that is calculated per device. Because of the process variations, the overall analog output span may exhibit variations from one device to another. Two otherwise identical devices may be perfectly linear, but with different overall output span from the minimum to the maximum different endpoints and step size values.

The DAC offset is defined as the difference between the ideal and actual analog output for a "zero code" digital input [7]. Some devices have a correction circuit to adjust offset voltage. The offset may be tested as a worst-case measurement when the correction circuit is disabled. The offset testing implies measurement of the analog output generated by the "zero code" input and comparison of the obtained value against the fault free case. Offset may be specified as a voltage, or a fraction of an ideal LSB step, or a percentage of the ideal reference level or FSR (Full-Scale Range). The example of the offset test plot is shown in Fig. 2.

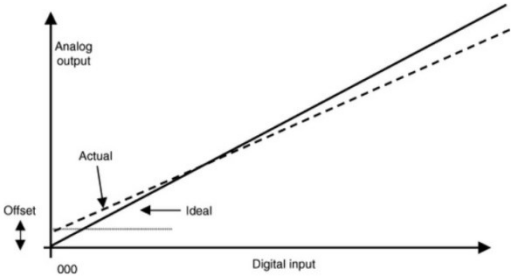

Fig. 2. Offset test plot

Gain is defined as the difference between the ideal and actual span of analog output values corresponding to the full range of digital input codes [7]. Because the total number of analog steps is $2^N - 1$, the ideal span is equal to the reference level (FSR), minus 1 ideal LSB step. The ideal LSB is equal to reference level divided by 2^N, so the span can be calculated as:

$$Reference\_level \times \left(\frac{2^N - 1}{2^N}\right) \quad (1)$$

The test procedure has to enable measurement of both the minimum output level (at "all zeroes"), and the maximum output level (at "all ones"), in order to determine the output span. The difference between the minimum and maximum output levels is specified as the device gain. DAC gain can be either positive (greater than the ideal), or negative (less than the ideal). The example of the gain test plot is shown in Fig. 3.

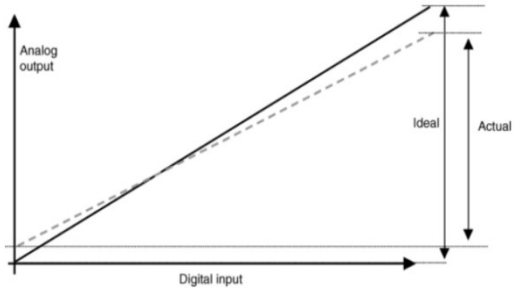

Fig. 3. Offset test plot

Ideally, each step of the DAC digital input value would increment the DAC analog output by exactly one step [7]. In an actual device, the analog step size varies. The range of the DAC describes the range of values from the minimum digital code (offset) to the maximum digital code (full scale). Linearity tests evaluate the transfer function (dependence of the output voltage levels from the input codes) based on the measured endpoints. The device LSB step is calculated by dividing the measured span of the DAC

by the number of possible input codes, as follows:

$$DeviceLSB = \left(\frac{Voltage[2^N-1]-Voltage[0]}{2^N-1}\right), \qquad (2)$$

where Voltage[N] indicates the device analog level with an input code of N.

Differential Nonlinearity (DNL) is defined as the difference between the actual step size and the calculated step size [7]. Integral Nonlinearity (INL) represents the worst-case variation in any of the analog output values with respect to an ideal straight line drawn through the endpoints of the I/O graph [7]. INL is also sometimes defined in comparison to a "best fit" straight line. The illustration of the differential and integral nonlinearities is shown in Fig. 4.

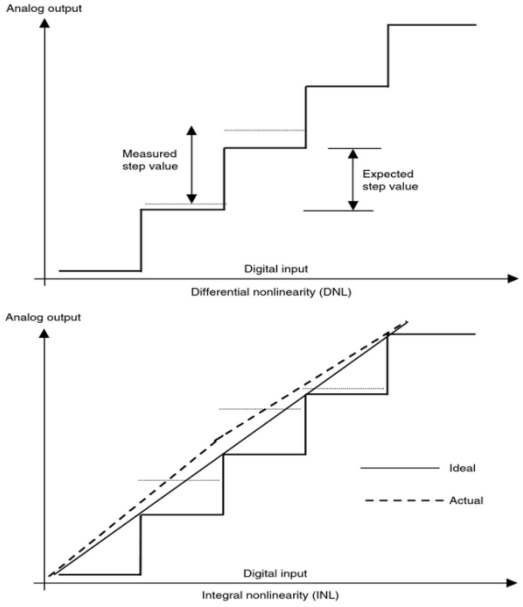

Fig. 4. Differential and integral nonlinearity

If only the DNL is tested, then each step could be "in spec", but the accumulated error could be excessive as compared to a straight-line transfer curve. If only INL is tested, then the device response according to a straight-line transfer curve could be acceptable, but each code step could exhibit excessive variation.

III. System Hardware

Digital to analog converter is used to generate analog voltage values that correspond to an input digital data [8]. Data in binary digital form can be converted into the corresponding analog form i.e. voltage value using a R-2R ladder (binary weighted resistor) network and a summing amplifier. In a mixed-signal system (analog and digital), a reconstruction (low-pass) filter at the output is used to smoothen the analog signal at the output of the DAC. The topology of such DAC circuit is shown in Fig. 5.

A basic R–2R resistor ladder network is shown in Fig. 6. Bit a_{n-1} (most significant bit, MSB) through bit a_0 (least significant bit, LSB) are driven simultaneously from a register circuit. Ideally, the input bits toggle between V = 0 (logic 0) and V = V_{ref} (logic 1). The R–2R network determines how much these digital bits contribute by their weights to the value of output voltage V_{out}. Depending on the input digital word, the output voltage (V_{out}) will have a corresponding discreet value between 0 and V_{ref} minus the value of the minimal step, corresponding to bit 0.

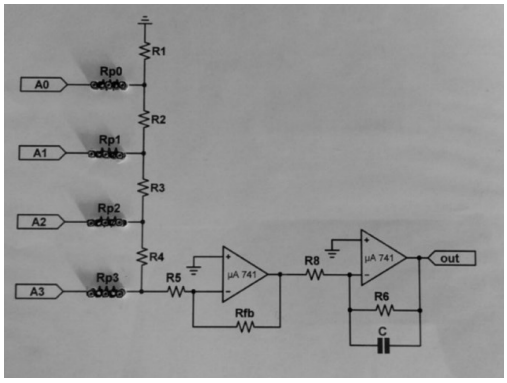

Fig. 5. Digital to analog converter using R-2R ladder network and summing amplifier, with reconstruction filter at the output

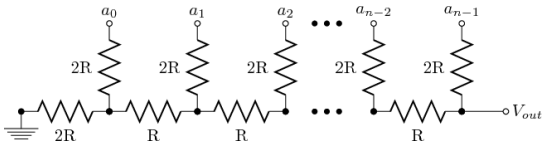

Fig. 6. n-bit R–2R resistor ladder

For a digital value VAL, of a R–2R converter with N bits and 0 V/V_{ref} logic levels, the output voltage V_{out} can be calculated as (3):

$$V_{out} = V_{ref} \times \frac{VAL}{2^N} \qquad (3)$$

In this case, if N = 4 (hence 2^N = 16) and V_{ref} = 3.3 V (typical CMOS logic 1 voltage), then V_{out} will vary between 0 volts (VAL = 0 = 0000_2) and the maximum (VAL = 15 = 1111_2):

$$V_{out} = 3.3V \times \frac{15}{2^4} = 3.09375V \qquad (4)$$

with steps (corresponding to VAL = 1 = 0001_2):

$$\Delta V_{out} = 3.3V \times \frac{1}{2^4} = 0.20625V \qquad (5)$$

Testing of the DAC can be performed by introducing catastrophic defects i.e. by changing the input resistances Rp_0, Rp_1, Rp_2 and Rp from zero to an indefinite value[3], and by recording the transfer curves for different cases. The defects can be categorized as parametric i.e. soft, or catastrophic i.e. hard. By observing the corresponding response of the DAC, one can learn about the effects of such defects to the shape of the transfer curve, linearities and accuracy of similar circuits.

IV. Software

LabVIEW programs are often referred to as virtual instruments, or VIs, because their appearance and operation imitate physical instruments, such as oscilloscopes and

multimeters. LabVIEW contains a comprehensive set of tools for acquiring, analyzing, displaying, and storing data, as well as tools for code troubleshooting.

NI High-Speed M Series is a high-speed multifunction data acquisition (DAQ) device that uses NI LabVIEW-based software instruments [9], which allows measuring and analyzing of real-world signals. This device provides up to: 8 analog inputs (differential, or 16 single-ended), 2 analog outputs, 48 digital inputs and outputs, 2 counters, power supplies, NI-PGIA 2 and NI-MCal calibration technology for improved measurement accuracy on a compact USB device.

Each VI has two components:

- Front panel, that is containing a GUI of the VI.
- Block diagram, serving as a work-space for graphical programming.

The user interface is shown in Fig. 7. When VI is created, it has a blank front panel by default. Afterwards, control and indicator elements are added to define the inputs and outputs of the system. In this case, the VI consists of several parts: STOP control which stops the virtual instrument, Boolean indicator for binary input, and a XY graph that displays the transfer curve of the DAC.

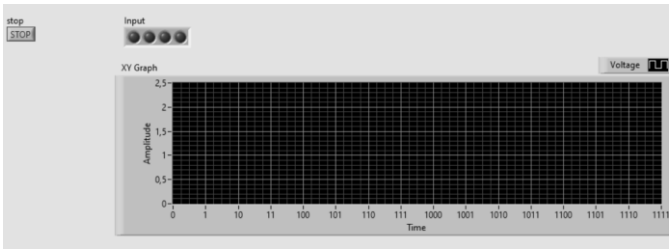

Fig. 7. User interface – front panel view

The block diagram contains the graphical source code of a LabVIEW program and it's shown in Fig. 8.

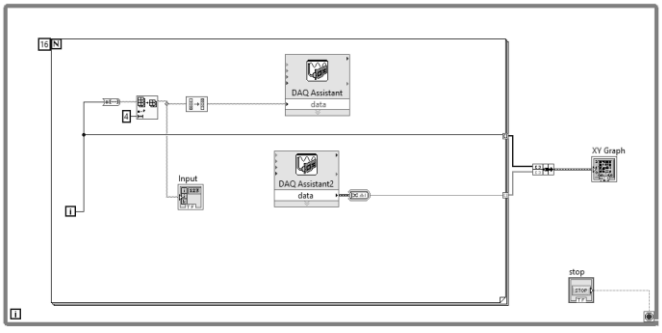

Fig. 8. Main thread – block diagram view

The concept of the block diagram is intended to separate the graphical source code from the user interface in a logical and simple manner. Front panel objects appear as terminals on the block diagram. Terminals on the block diagram reflect the changes made to their corresponding front panel objects and vice versa.

V. Results

The correctness of the realized circuit is determined by putting the actual circuit into operation. Physical realization of the project and the results of measuring are shown in figure 9. A part of a mock-up of the converter circuit is shown in Fig. 5. Some of the resistors from the schematic could be replaced with wires or left unconnected or varied in order to imitate the presence of the fault in the circuit. Each measurement implies graphical representation of the transfer curve that can be further analyzed for assessing the performance of the converter or studying the effects of different defects in the circuit.

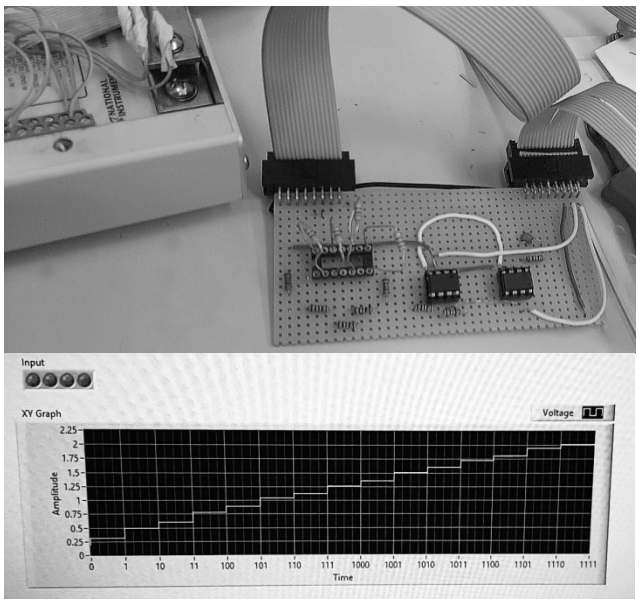

Fig. 9. D/A converter PCB connected with the DAQ and results of measuring

VI. Conclusion

The aim of the paper was to implement and study the operation of D-to-A converters as well as the effect of different types of defects, that could appear in this circuit. It is intended for educational purposes. It is supported by hardware and software co-design, and will be used for conducting laboratory excesses in Mixed-signal circuit testing.

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